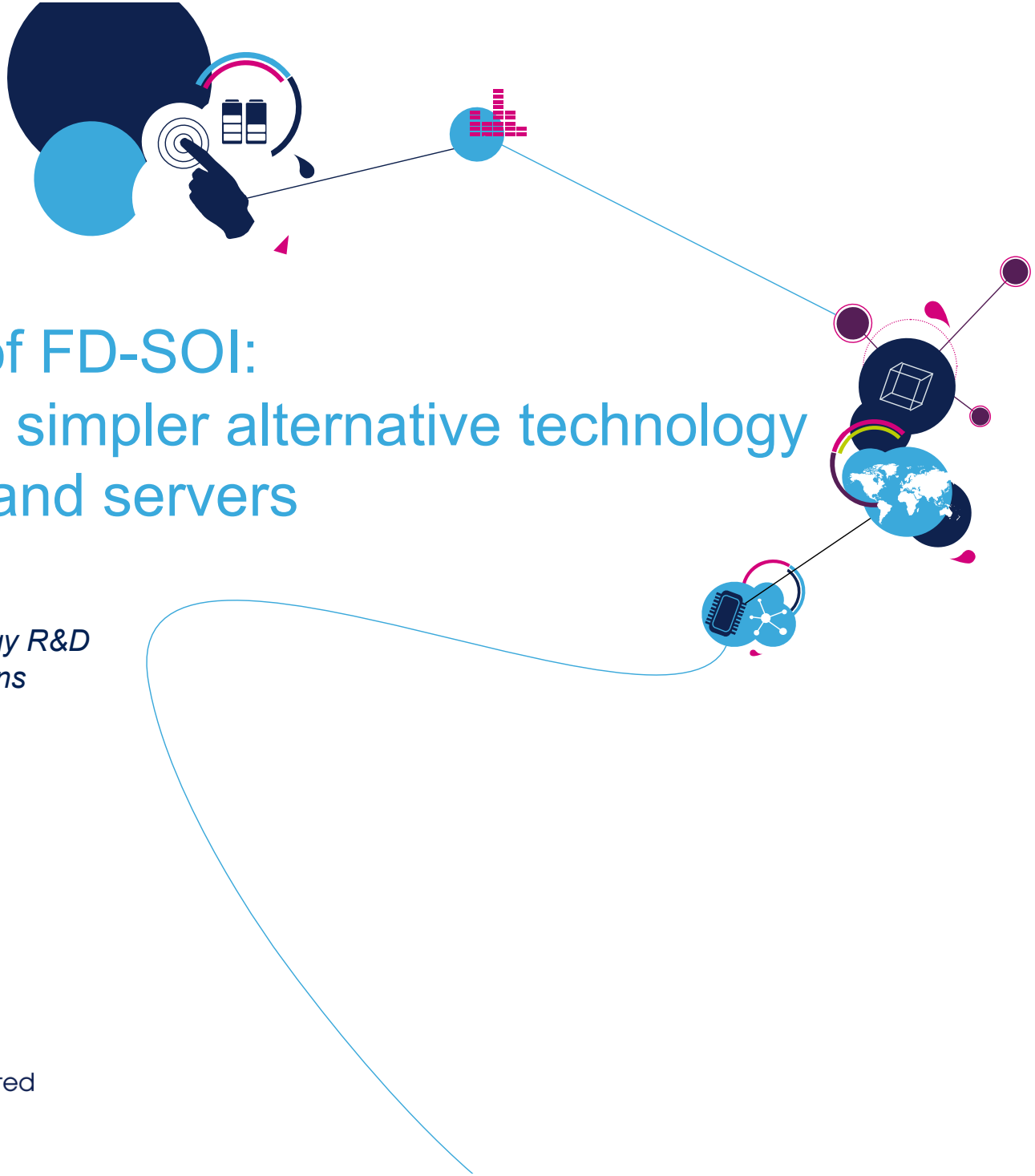
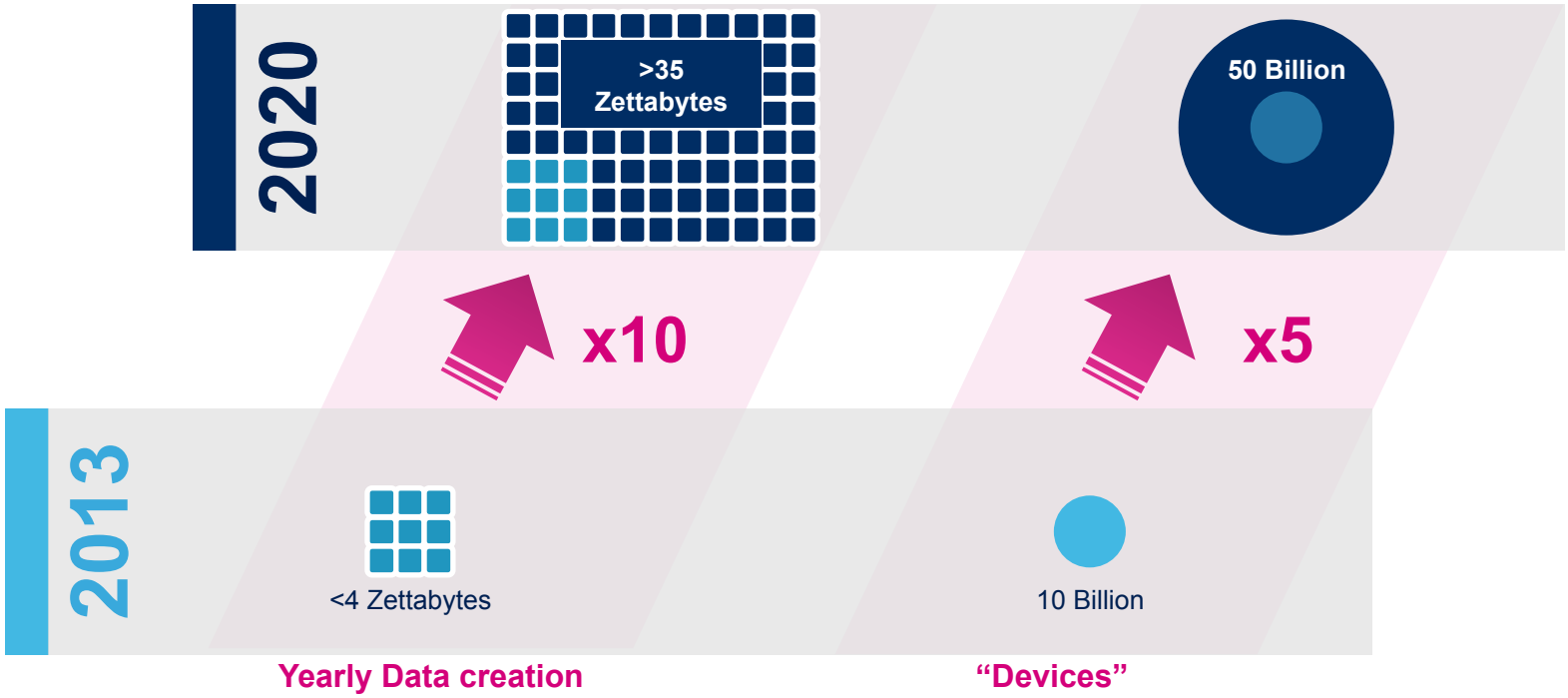


A brief history of FD-SOI: a faster, cooler, simpler alternative technology for IoT, mobile and servers

Giorgio Cesana
FE Manufacturing & Technology R&D
Embedded Processing Solutions
STMicroelectronics

life.augmented

The Digital Explosion



A Zettabyte = 10^{12} Gigabytes

Digital Market Dynamics

Cloud & Network infrastructure

Traffic & storage explosion driving

- Cloud storage & server
- Core network
- Radio access network

Technology impact

- Network architecture
- Higher integration & performance
- Power efficiency
- Reliability

Hubs, Gateways, Application Processors Connected devices & things

Explosion of connected devices

- Mobility / Smartphones
- Internet of things
- Autonomous devices

Technology impact

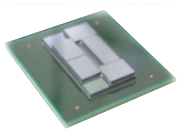
- Power Autonomy
- Ultra low power sensors
- Integration Digital, RF, Power Management
- Higher performance at lower power

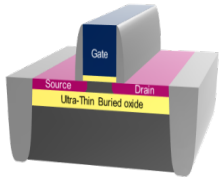
Explosion in connected “devices” & associated digital content creates a global power challenge

The various aspects of power efficiency

Silicon & Packaging Technologies

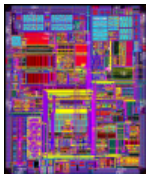
Performance/Power Efficiency & Density





FD-SOI

Heterogeneous architecture



- Multicores
- Scaleout computing
- Dedicated accelerators

System architecture

System Power Management

Design technics

- Use case analysis
- Clock gating
- DVFS, Power domains
- Software power management

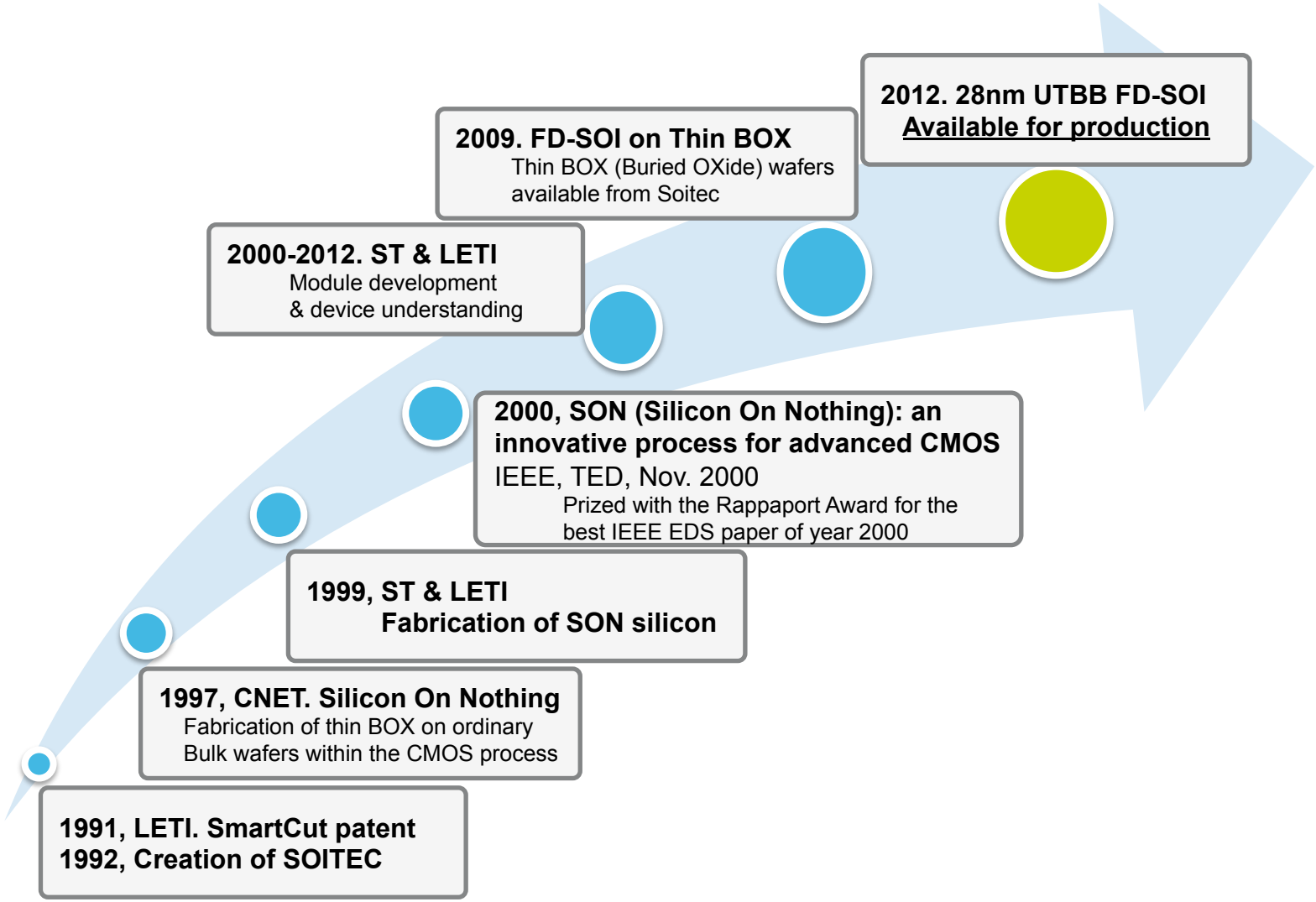
Energy Harvesting

Convert heat, movement, light into electricity

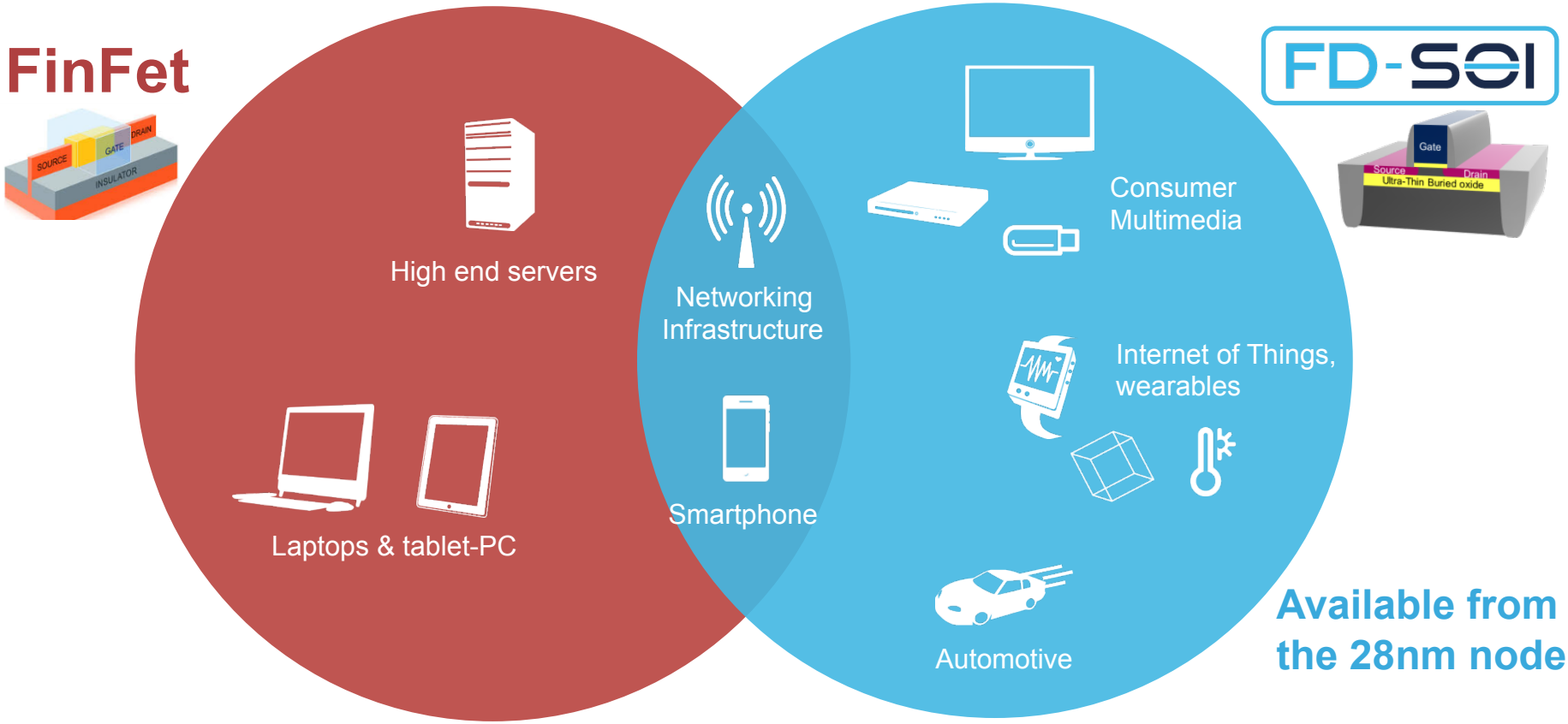
Energy harvesting

FD-SOI Technology

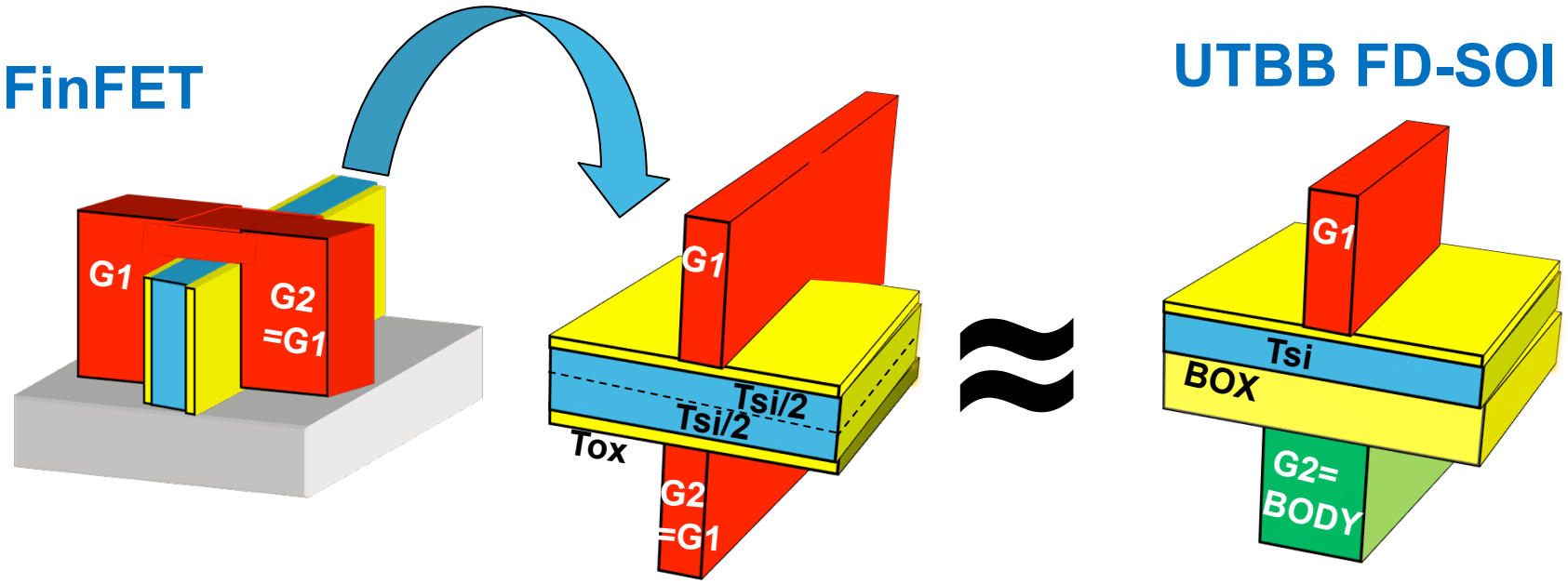
UTBB FD-SOI, A Long R&D Success Story



FD-SOI addressing Power sensitive Markets

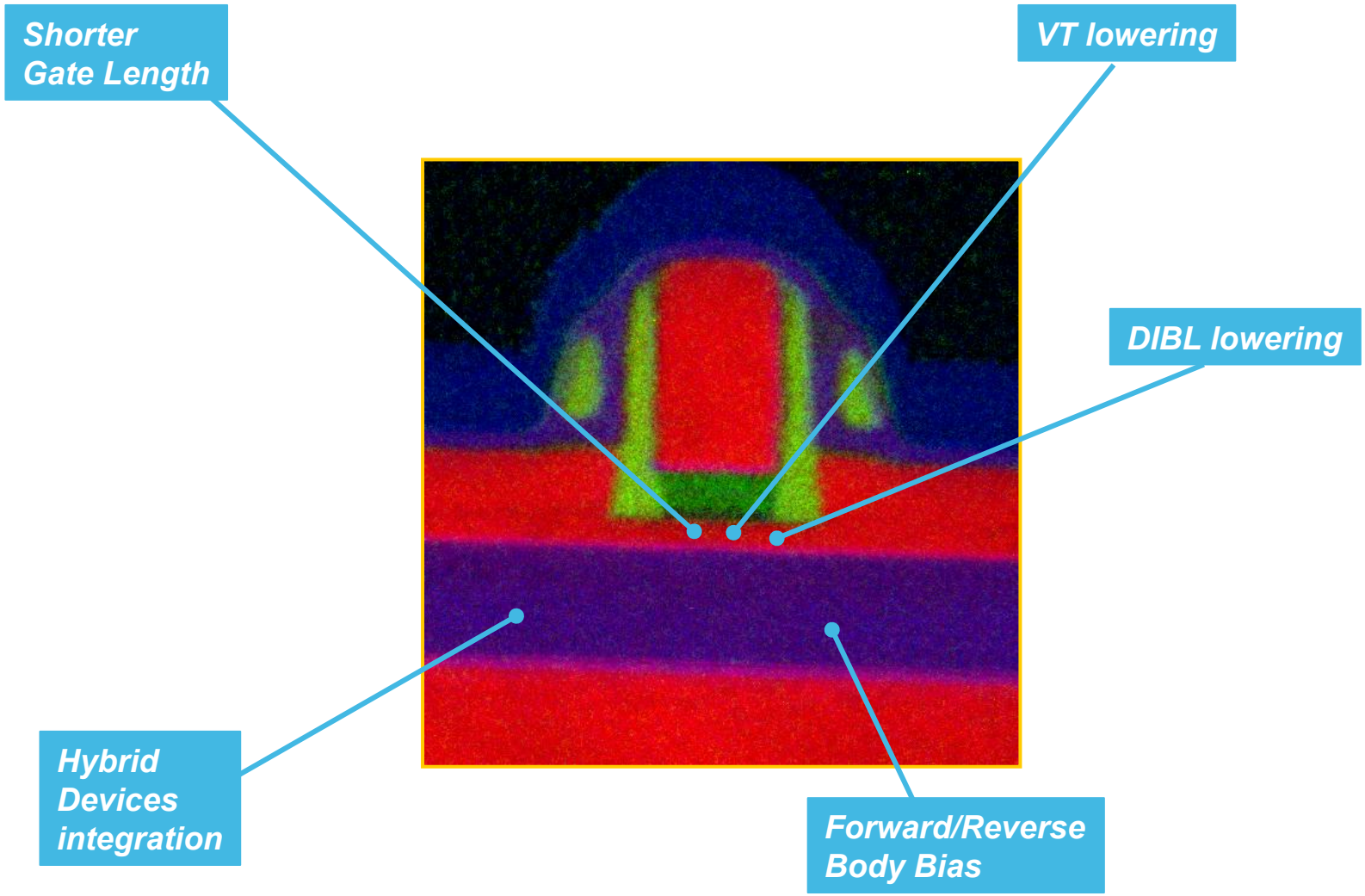


Fully Depleted Transistors

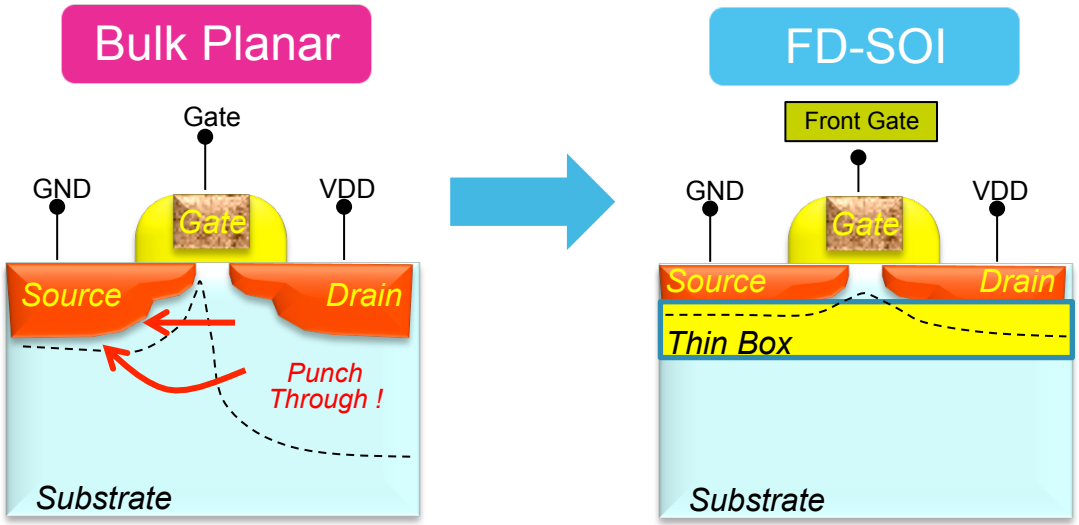


FinFET and UTBB SOI look like one another: just a rotation
Ultimately they converge to the same structure when scaling BOX to TOX

FD-SOI Transistor Summary



FD-SOI Electrostatics



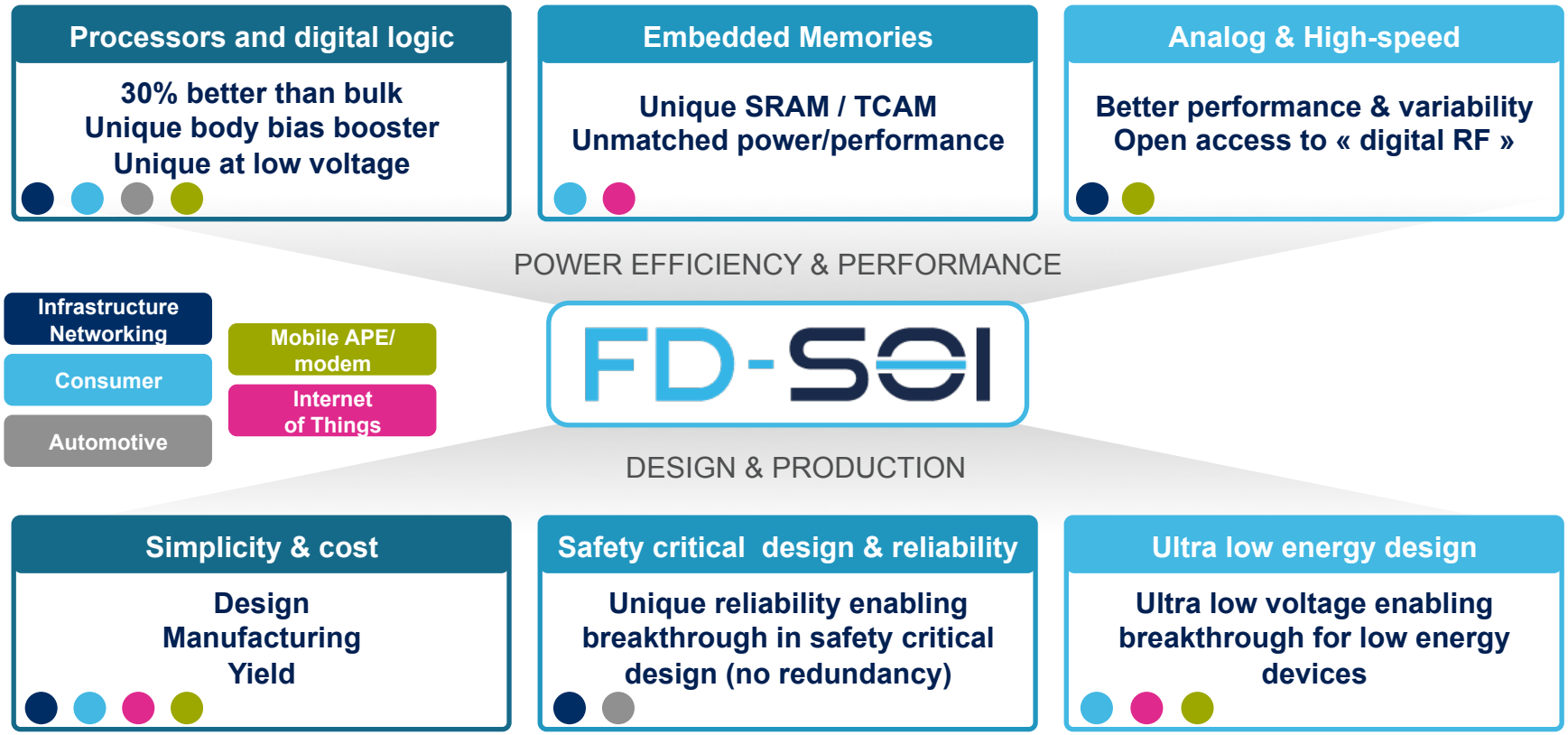
Bulk → $DIBL = 0.8 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{X_j^2}{L_{el}^2}\right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{ds}$

FD-SOI → $DIBL = 0.8 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{T_{Si}^2}{L_{el}^2}\right) \frac{T_{ox}}{L_{el}} \frac{T_{Si}}{L_{el}} V_{ds}$

Si film thickness replace junction depth (Xj)

- Short Channel effects controlled by the Silicon Film thickness
  - DIBL reduced ➔ for same I_{off} : V_{tlin} is lower, I_{eff} is higher

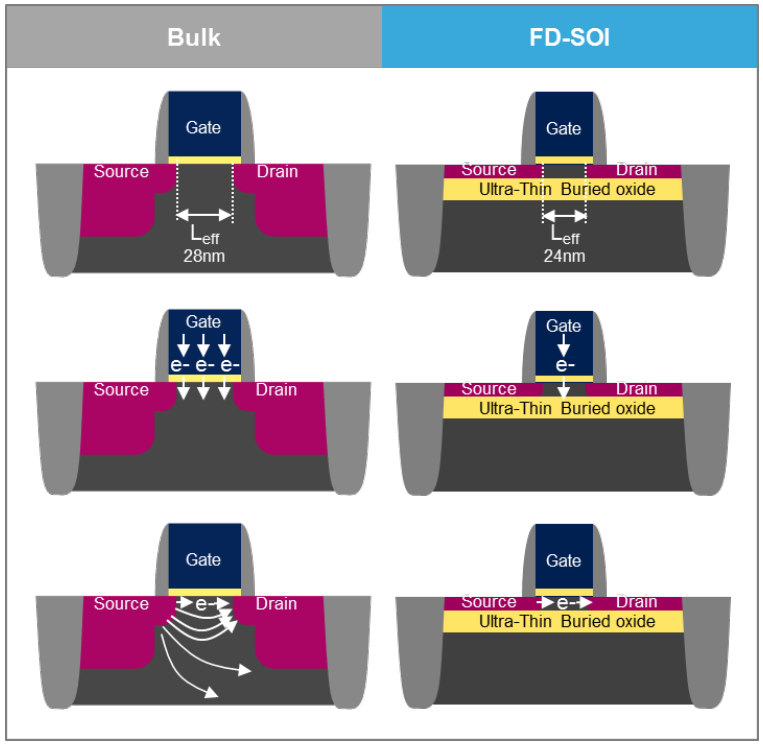
FD-SOI: unique value proposition



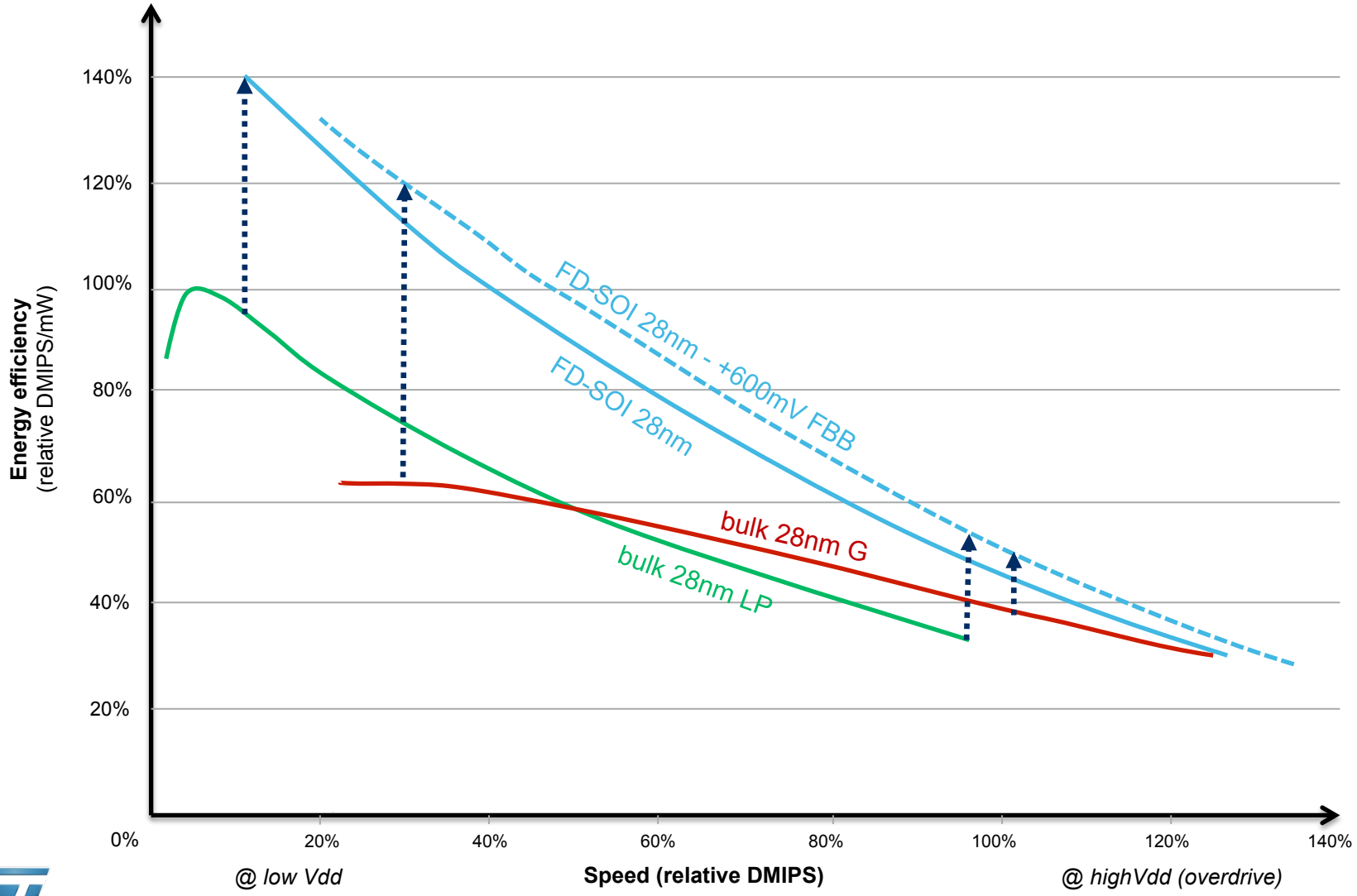
FD-SOI Technology Benefits

Efficient FD-SOI Transistors

- FD-SOI enables better transistor electrostatics
  - Enabling faster operation at low voltage, leading to better energy efficiency
  - Improving transistor behavior, especially at low supply, enabling ultra-low-voltage operation
  - Reducing transistor variability sources
- FD-SOI has a shorter channel length
  - Confirming scalability of the technology
- FD-SOI has lower leakage current
  - Lower channel leakage current
    - Carriers efficiently confined from source to drain
  - Thicker gate dielectrics, leading to lower gate leakage
  - Enabling ultra low power SRAM memories
  - Leakage current is less sensitive to temperature with FD-SOI



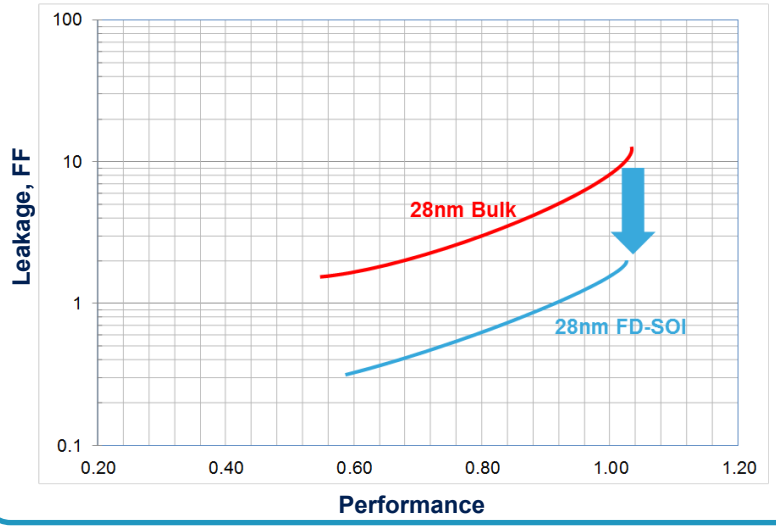
28nm FD-SOI Best in class efficiency



FD-SOI – Efficiency at all levels

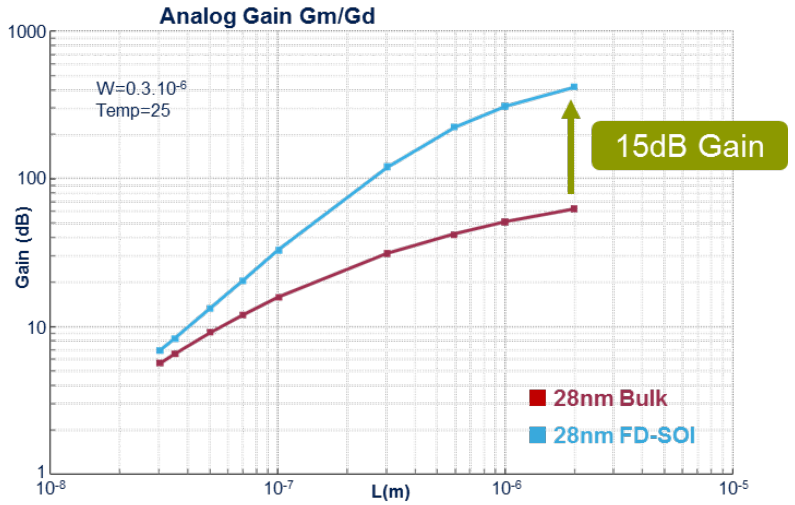
Memories

- Similar performance with huge ~5X less leakage in 28 FD-SOI vs. Bulk
- Very low neutron-SER SRAM, 100× better than bulk
- Alpha quasi-immunity → cost savings for packaging



Analog & High-speed

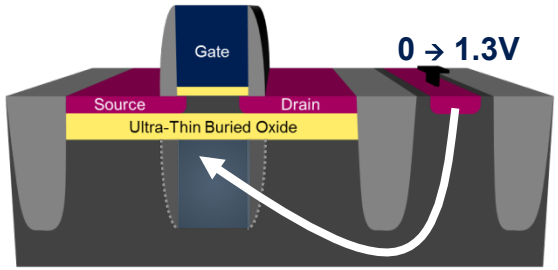
- FD-SOI analog performance far exceeds Bulk
- New design opportunity by controlling analog device characteristics through body biasing techniques



Forward Body Biasing (FBB)

A very reasonable effort for extremely worthwhile benefits

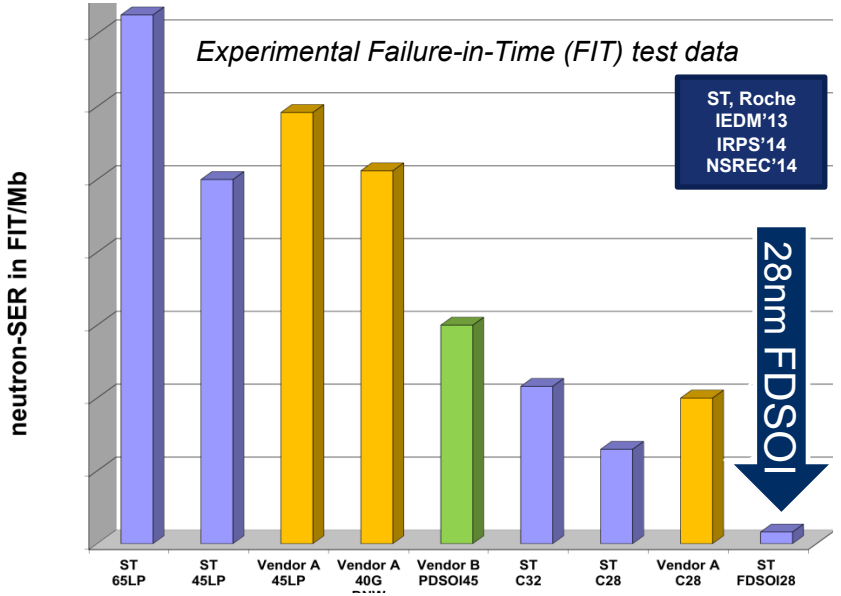
- An **extremely powerful** and flexible concept in FD-SOI to :
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts



- Comparatively **easy to implement** – if you've ever done DVFS you'll have no difficulty with Body Biasing

Best SER (Soft Error Rate) with FD-SOI

- Very low neutron-SER <10 FIT/Mb
  - ECC-SRAM not systematically required
  - standard FF intrinsically robust <10 FIT/MFF
  - rad-hard FF libraries available = 0 FIT
- Single Event Latchup immunity
  - tested with space ions 125°C/1.3V
- Alpha quasi-immunity <1 FIT/Mb
  - no need for ultra-pure alpha packaging
- Very small error clusters: 99% single bits
  - Single Error Correction efficient/sufficient
  - no need for bit scrambling as for BULK



Gain w.r.t. BULK	UTBB FDSOI	FinFET
Alpha	**1000×**	**15×**
Neutron	**100×**	**10×**
Latchup	**immune**	**not reported**
Multiple Cell Upsets	**99% single bit** max. 2 cells	**max. 4 cells** worse according to INTEL

ST, Roche, CISCO SER workshop, Oct'14

TSMC, Fang, CISCO SER workshop, Oct'14

FD-SOI Benefits
Application Examples

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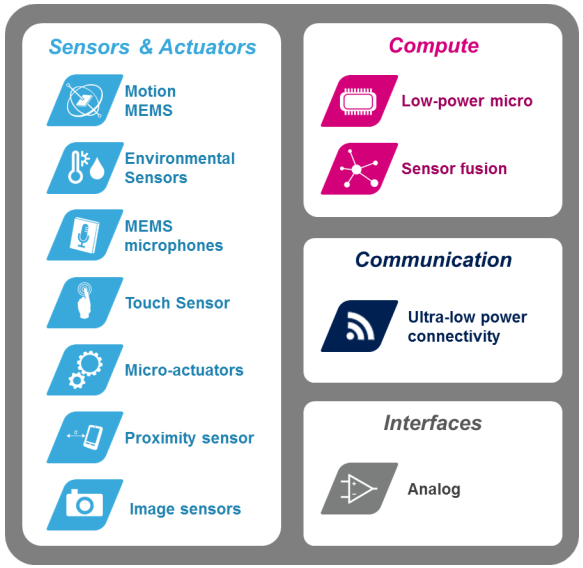
FD-SOI benefits for Internet of Things



Internet of Things

FD-SOI benefits for IoT

- Ultra low voltage / sub-threshold
- Low cost
- Integration RF/connectivity, micro, power management

Smart Car

Smart Home

Smart Me
Health / wellness

Smart City

Smart Industrial

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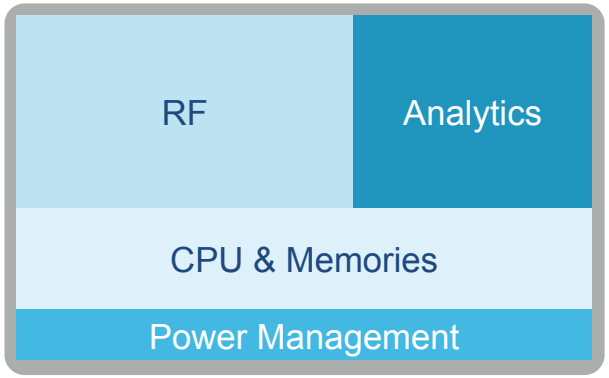
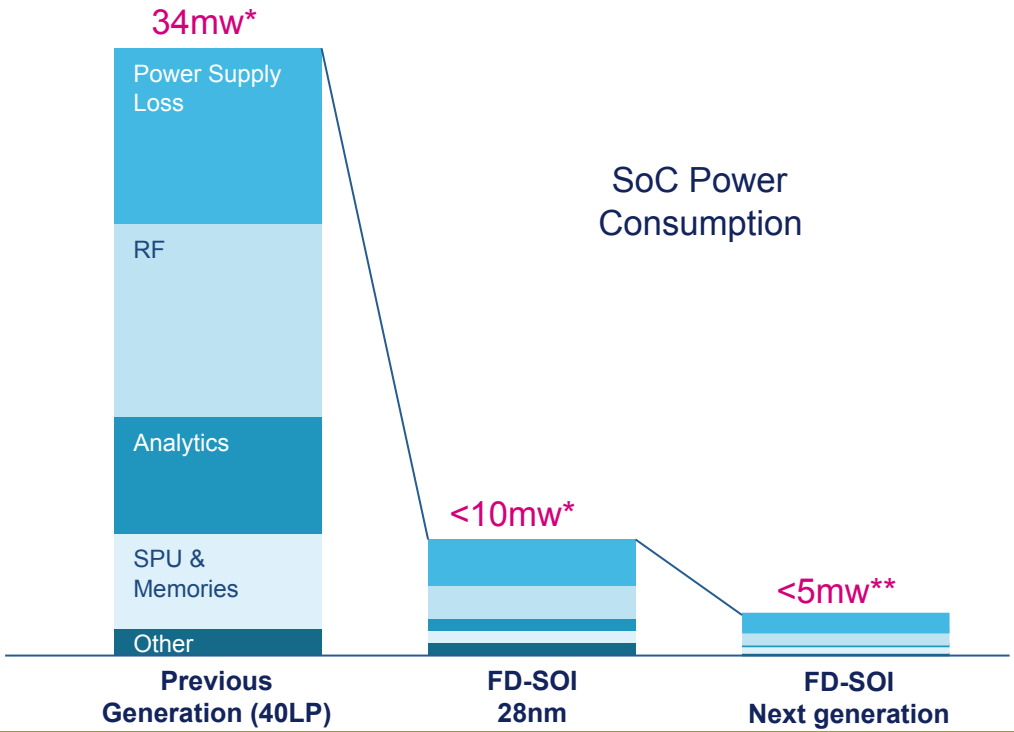
Example: Ultra Low Power in IoT

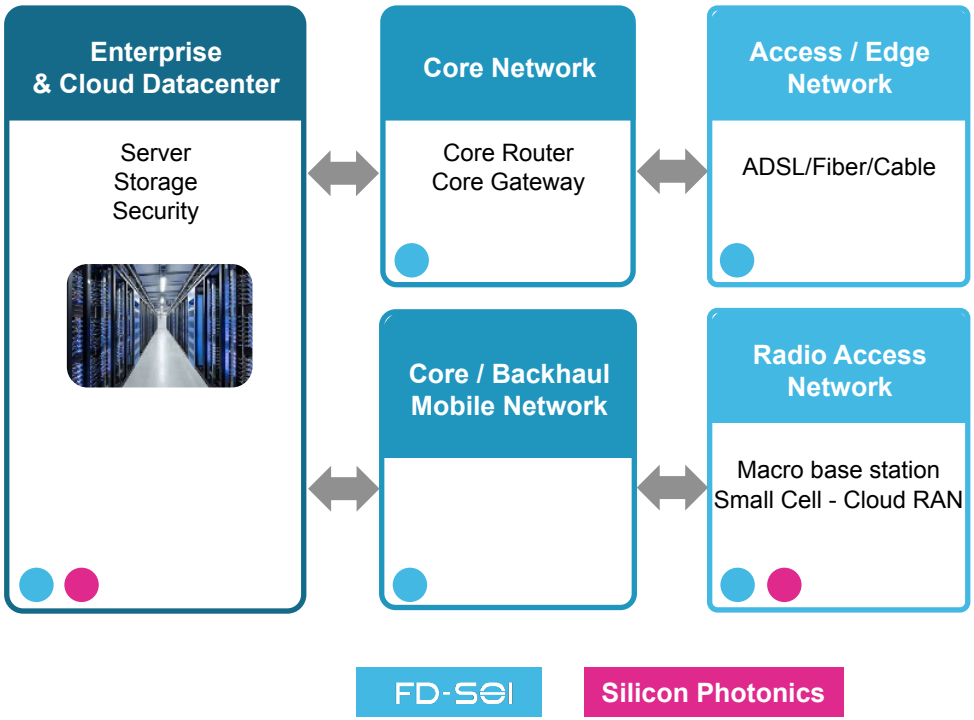




X3 to X6 Power Consumption Improvement with FD-SOI

* Measured on Silicon / Product Simulation
** Projection

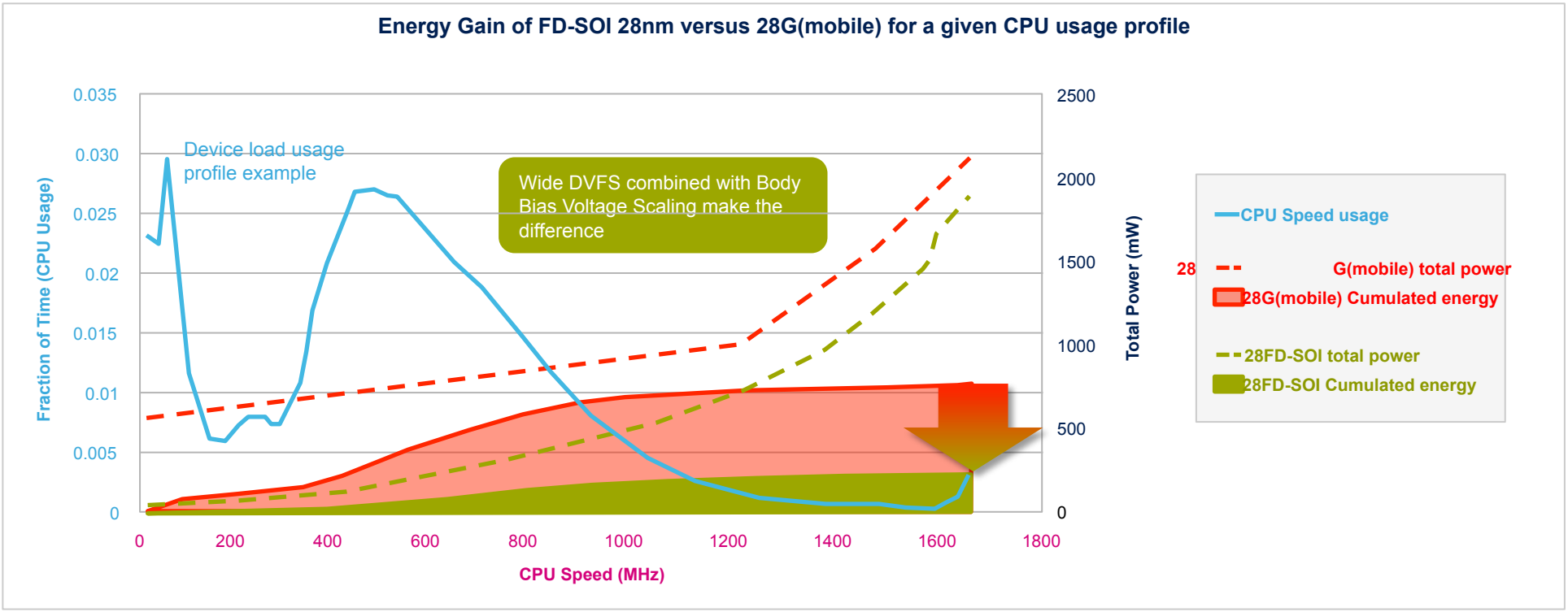
FD-SOI benefits in network infrastructure



FD-SOI benefits

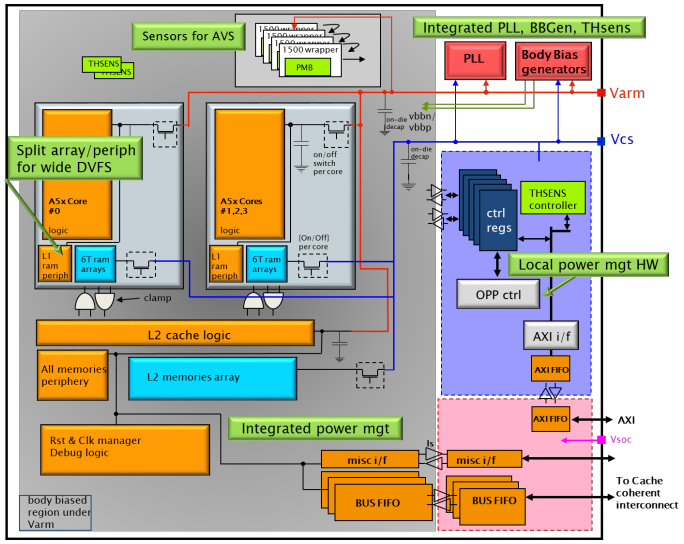
- Power efficiency
- Adapt power consumption to load
- Design complexity similar to previous nodes
- Applicable to all network infrastructure products
- Scalable down to FD-SOI 14nm

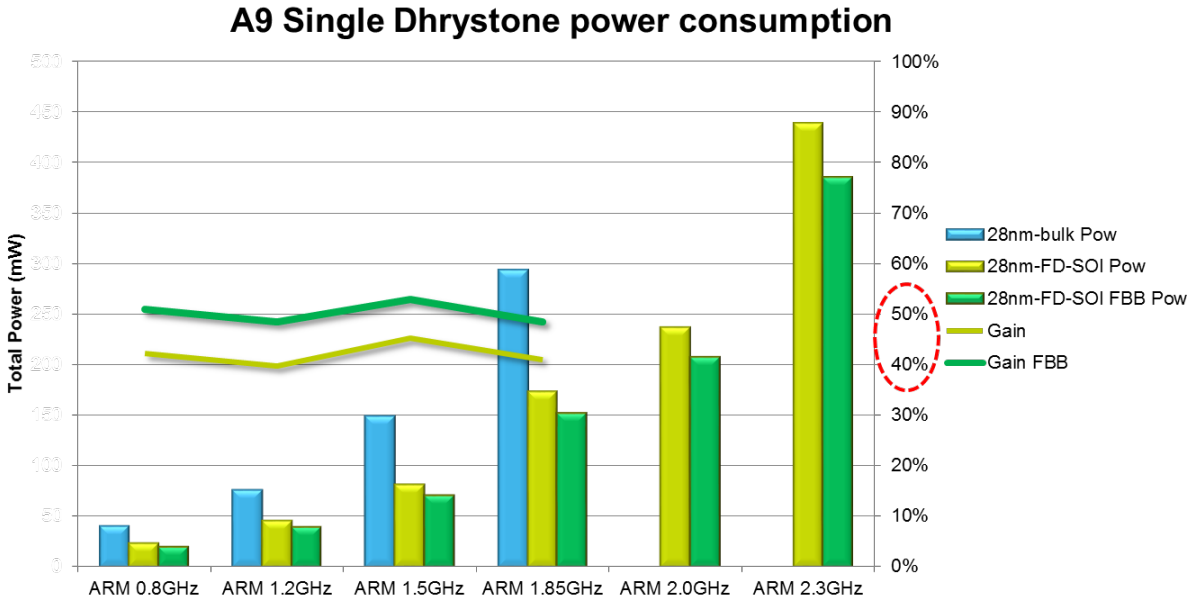
Example: Power efficiency in Mobile Infrastructure



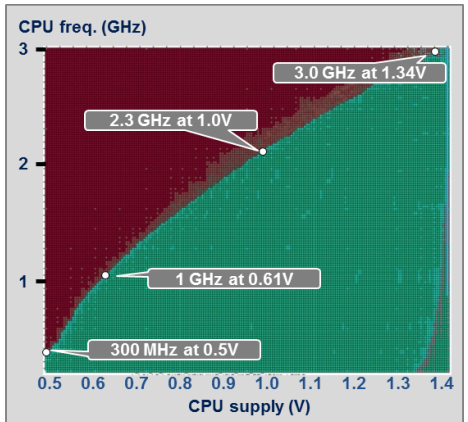
FD-SOI : up to 70% better energy consumption vs. 28nm bulk

Example: Power efficiency in APUs



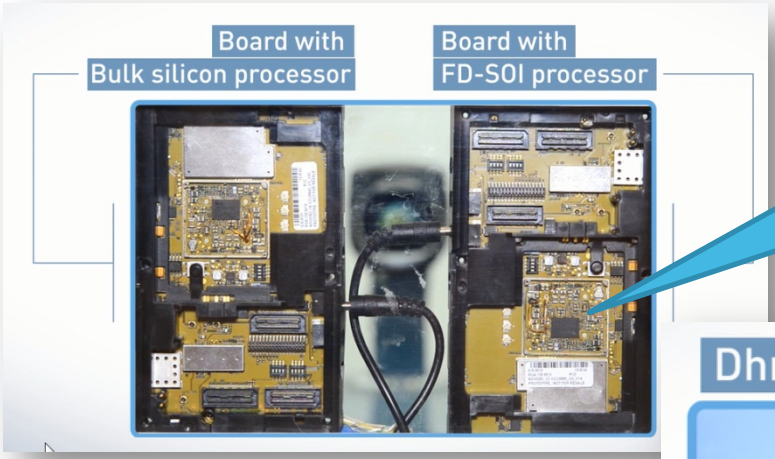


- FD-SOI allows the widest Vdd range for voltage scaling
- Still guaranteeing top notch speeds at very low operating voltage
- DVFS energy efficiency optimization is further extended thanks to body bias
  - Allowing to balance and optimize the static and dynamic power consumption components



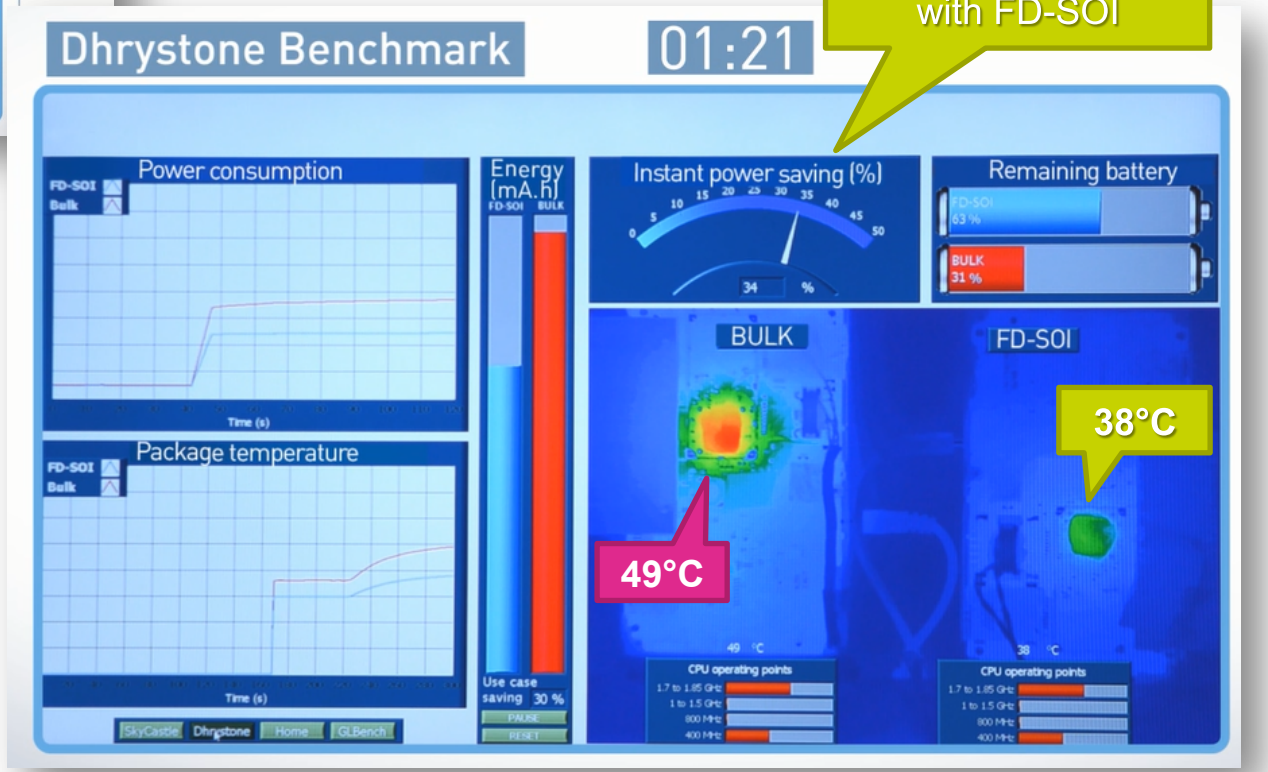
Real measurements of continuous DVFS in the range 0.5V – 1.4V

APU Cooler Demo: Si evidence



Same APU surface (28LP HKMG & 28nm FD-SOI) running Dhrystone bench at same 1.85GHz frequency

35% less total power with FD-SOI



At same speed, 28FD-SOI is 11° C **less** than 28nm bulk.

FD-SOI:
The Body Bias benefit

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How to improve Energy Efficiency?

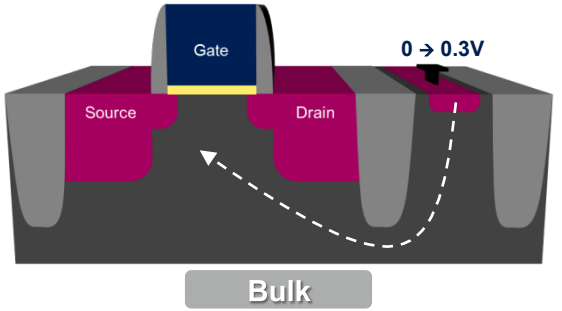
- Several technics exists but bulk process limit their efficiency in advanced nodes (28/14nm)

Technique	Limitations in Bulk
Increasing the # of processing cores	• leakage current for a given performance • limited DVFS
Wide range DVFS	• [Vmin, Vmax] range is limited by variability • Performance degradation when supply V reduces • Memory Array minimum voltage
Dynamic transistor Vt control	• limited body bias range • limited benefit in 28 nm / no benefit beyond
Poly biasing of the transistors	• limited poly biasing range

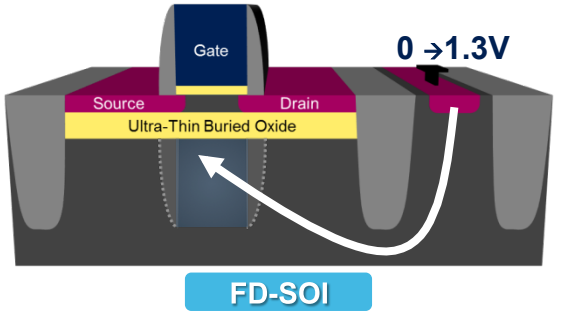
- New process & design technics are needed

FD-SOI: The FBB advantage

- What is Body Biasing?
  - A voltage is applied to the substrate (or body).
  - When voltage is positive, it is called **Forward Body Biasing**, or **FBB**



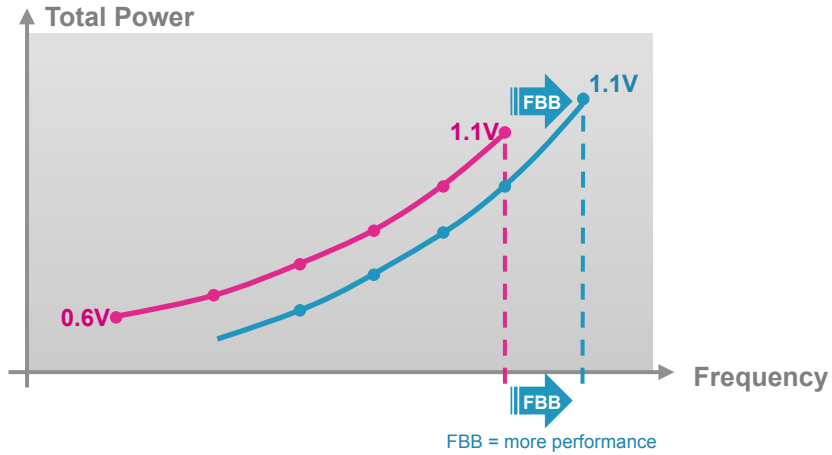
- Why FBB is much more efficient in FD-SOI?
  - The Insulator layer (UTTB) prevents the parasitic effects that normally appear during the body biasing
  - This allows much wider range of biasing compared to Bulk
  - FBB can be modulated dynamically during the transistor operation and the transitions are transparent to the SW



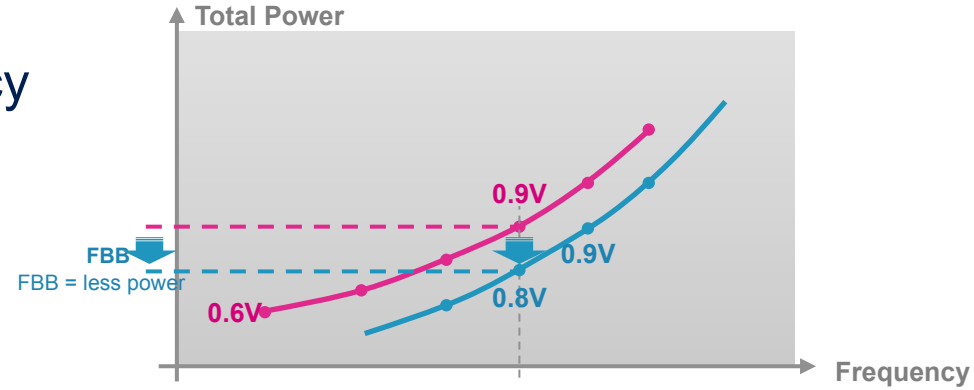
- FBB benefits
  - **Performance boost**
  - **Reduce power consumption** at a given performance requirement
  - **Process compensation** reducing the margins to be taken at design
  - **Easy to implement**: seamless inclusion in the EDA flow

FBB for performance boost and power efficiency

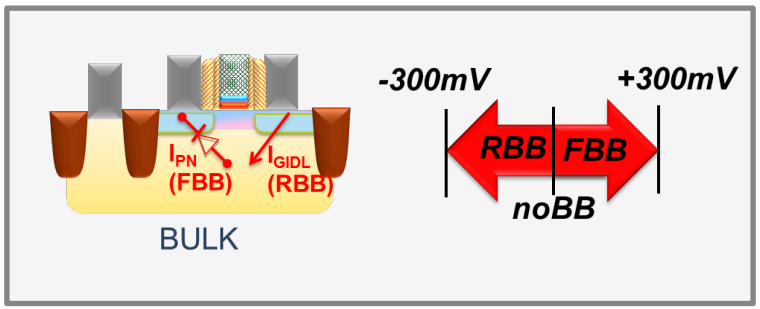
- FBB provides performance boost when voltage can't be increased
  - Limited impact on dynamic power, no impact on voltage drops
  - → More efficient performance increase than turning the voltage
  - Impact on leakage at high temperature
  - Back into 28G range but leakage can be turned off anytime by removing FBB



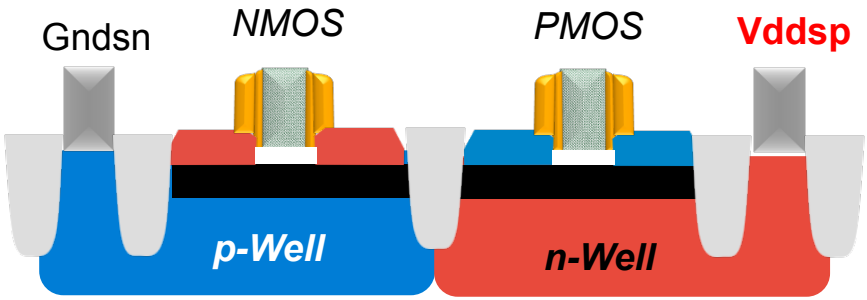
- FBB improve the power efficiency at a given frequency
  - Limited impact on leakage, slightly higher than without FBB
  - Drastically decrease dynamic power

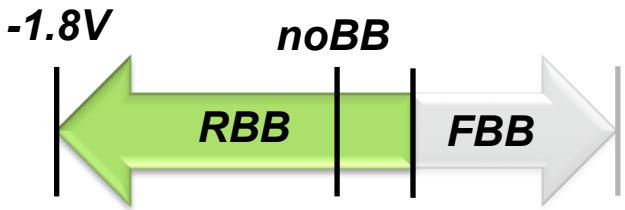


FD-SOI: LVT & RVT Body Bias range



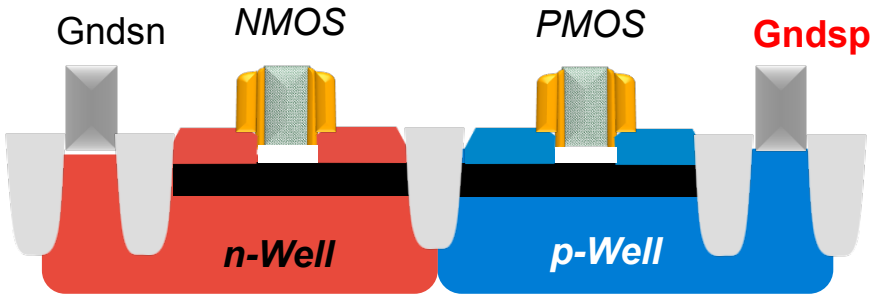
RVT : Conventional Well (CW) - RBB

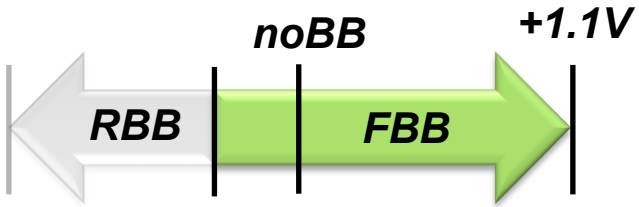




Vdd/2+ 300mV

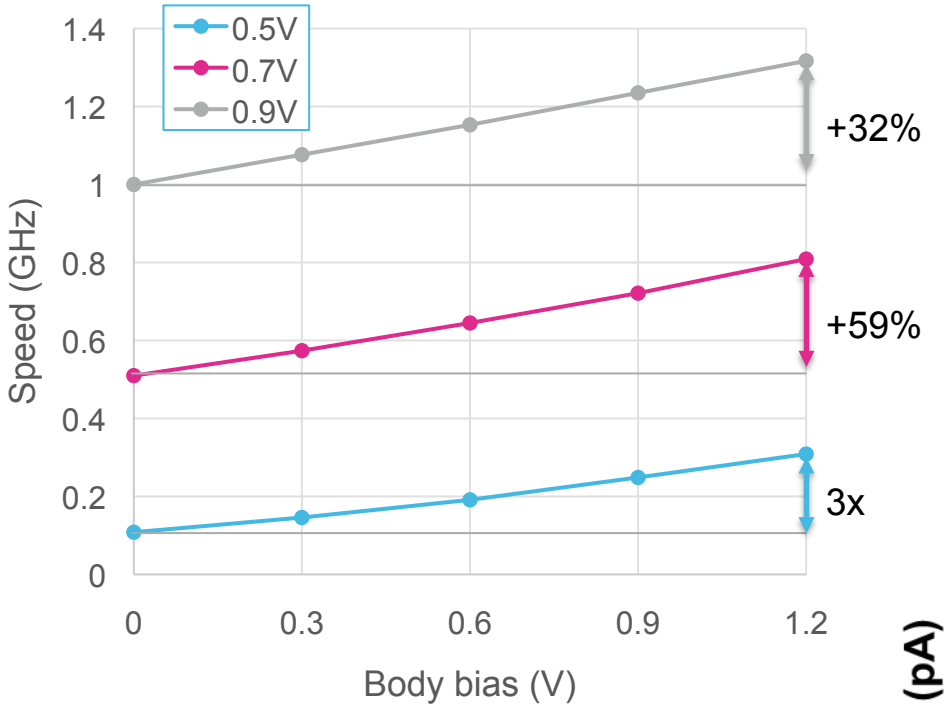
LVT : Flip Well (FW) - FBB





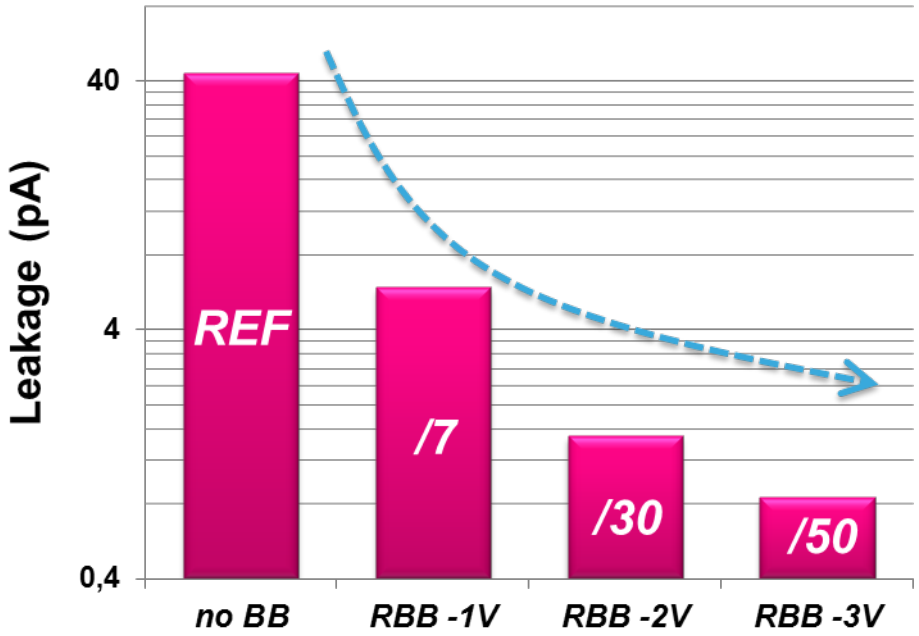
-300mV

Body Bias Efficiency



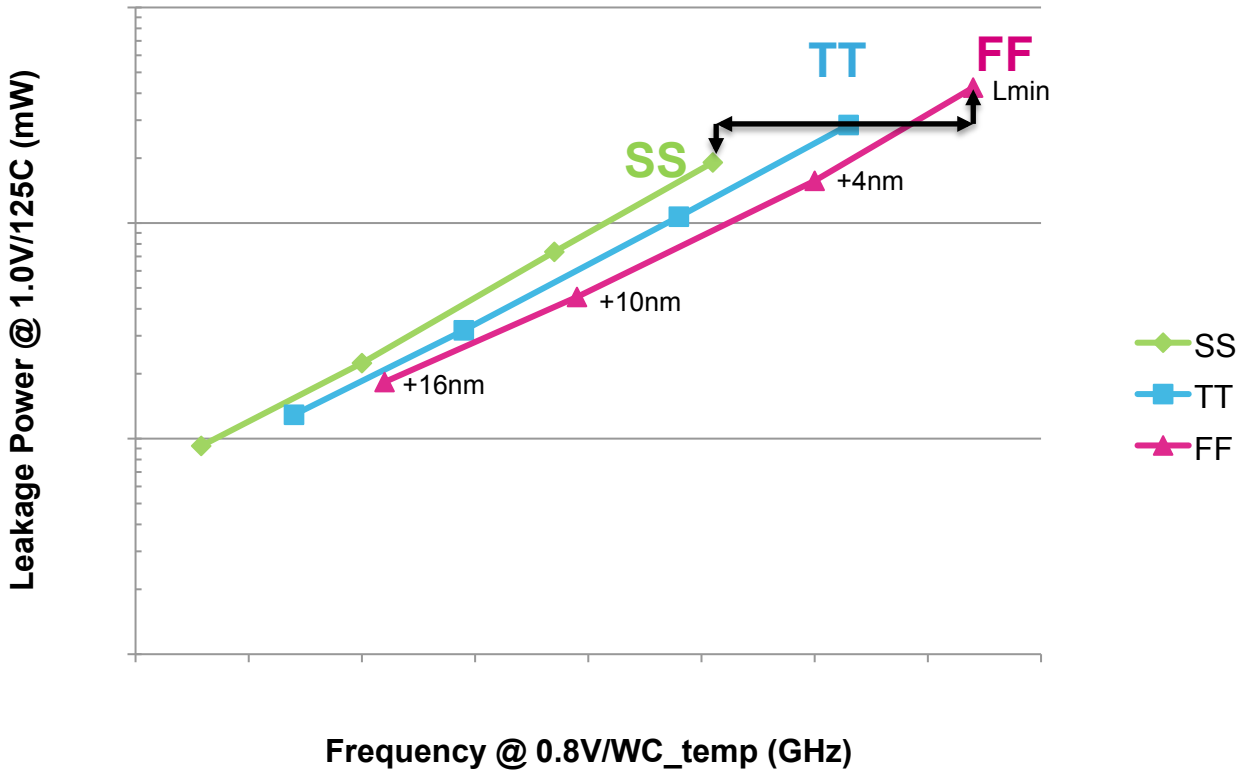
LVT / Forward Body Bias

RVT / Reverse Body Bias



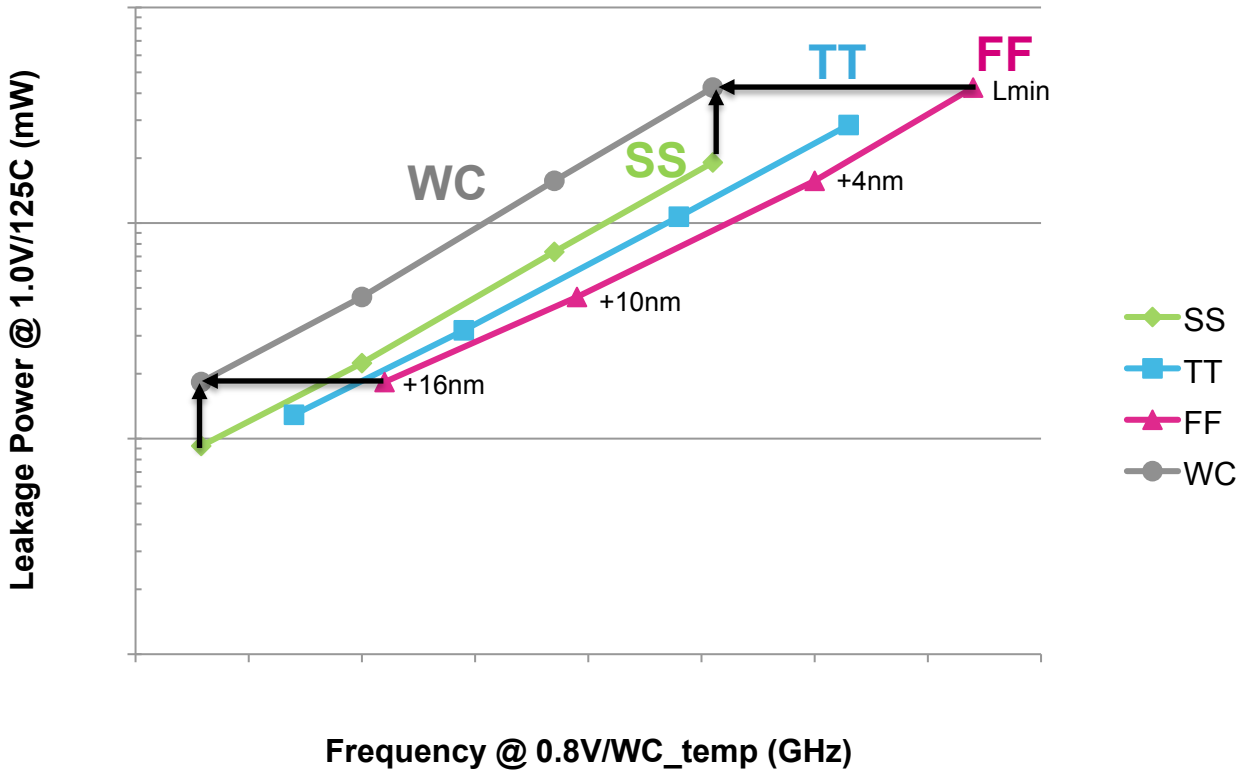
Process Compensation with Forward Body Bias (FBB)

Performance Corner Spread w/o Body Bias



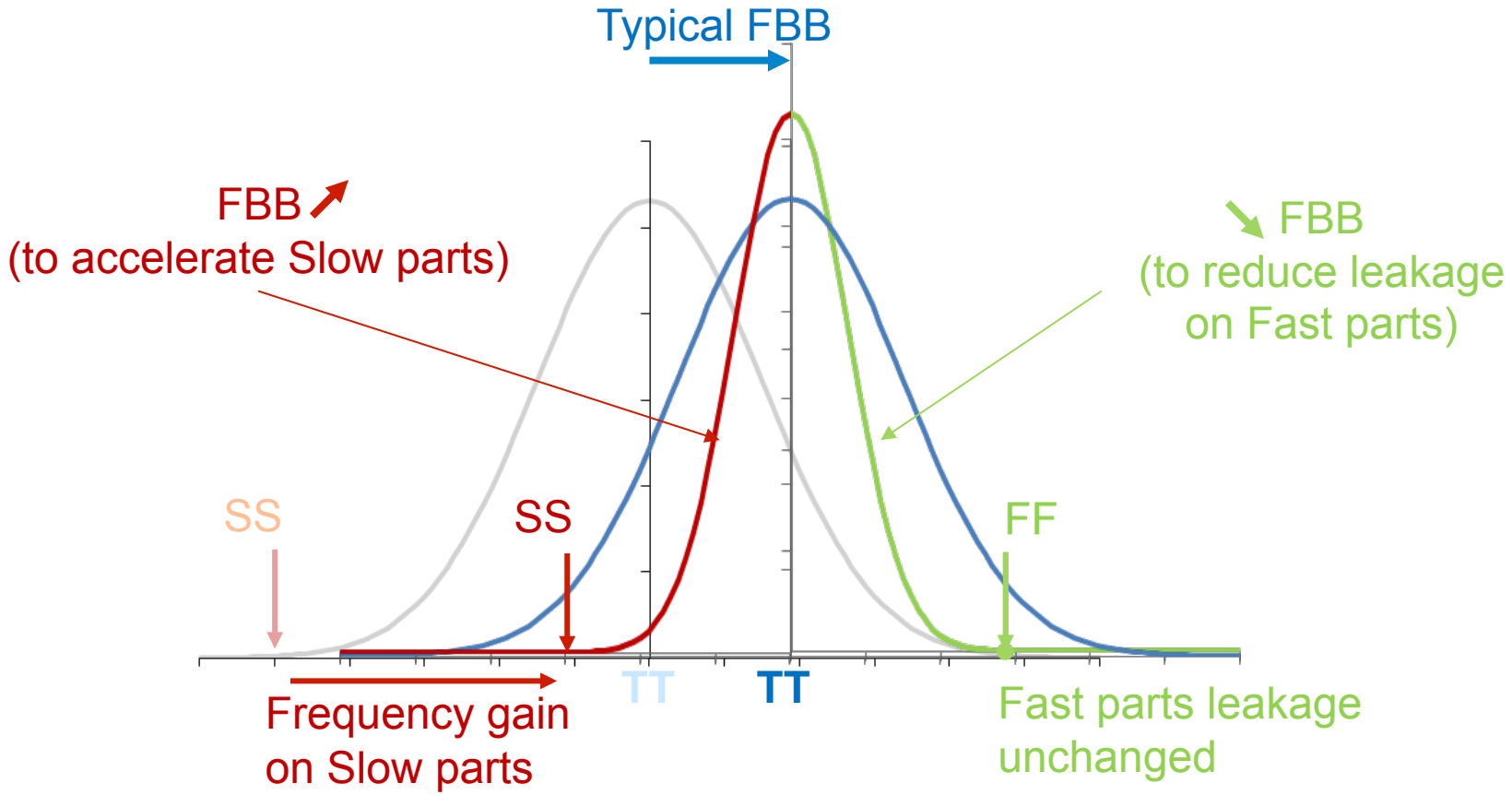
- Frequency and leakage corner spreads depend on PVT and channel length

Worst Case Performances w/o Body Bias



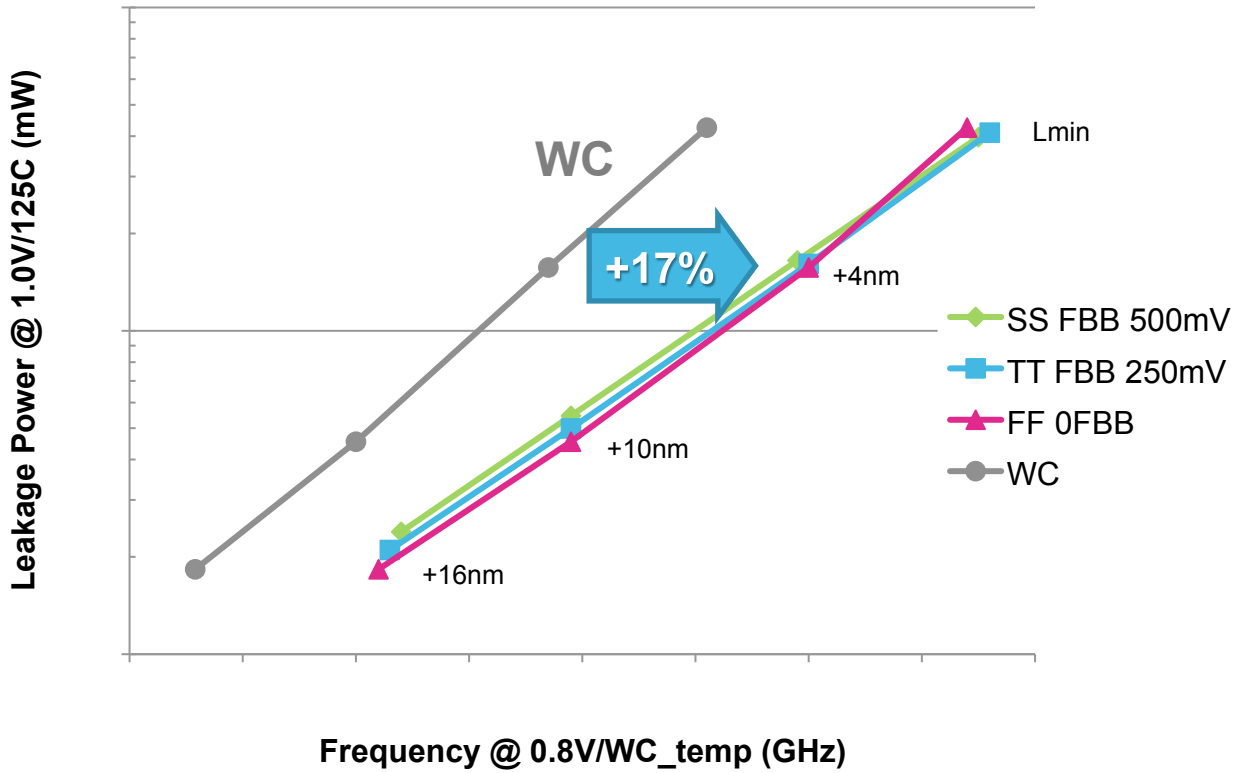
- For each gate length, the worst case performance trend (WC) is built using the slowest case (SS) and the leakiest case (FF)
- This is what used for ASIC sign-off

FBB-based Process Compensation: Principle



- SLVT doesn't allow RBB → FBB must be applied on typical to allow "pseudo-RBB" for Fast parts (leakage containment)
- Higher FBB is applied to accelerate Slow parts

Process Compensation Through FBB

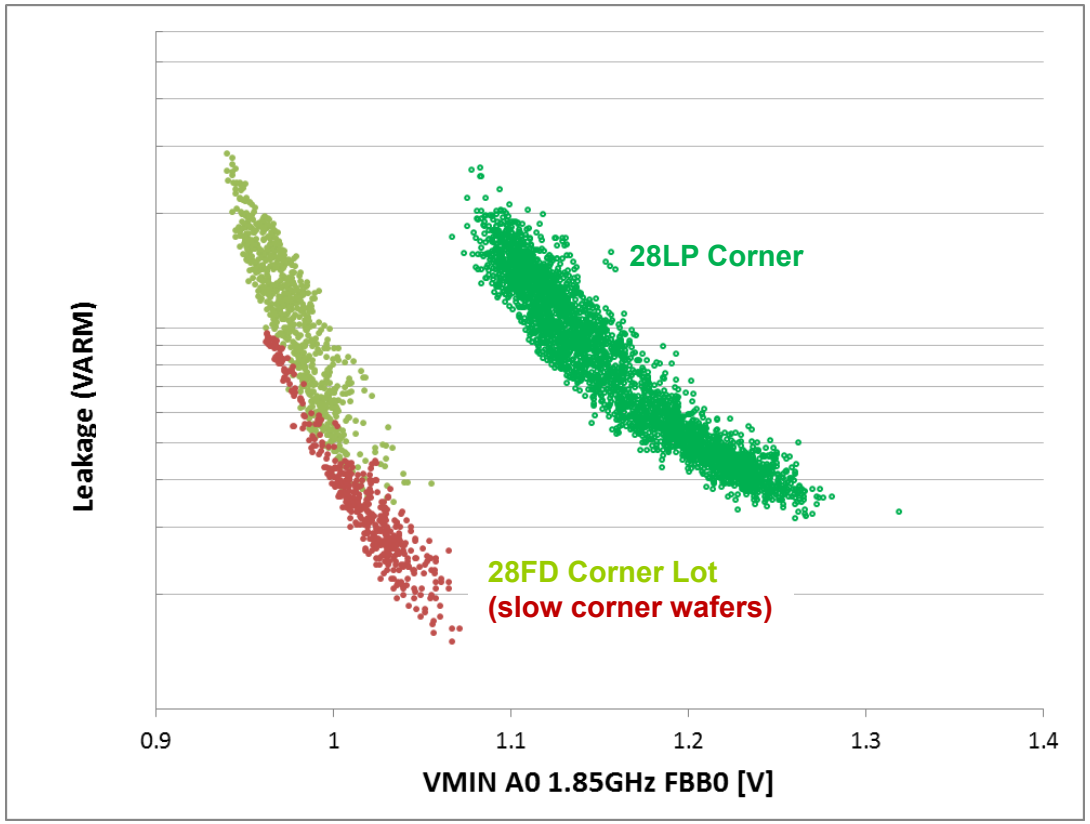


- Process Compensation through FBB allows
  - Masking SS-FF process spread
  - Recovering +17% speed in 28nm FD-SOI, at no dynamic power expense (as it would happen if using AVS)

FBB: a “true” process compensation

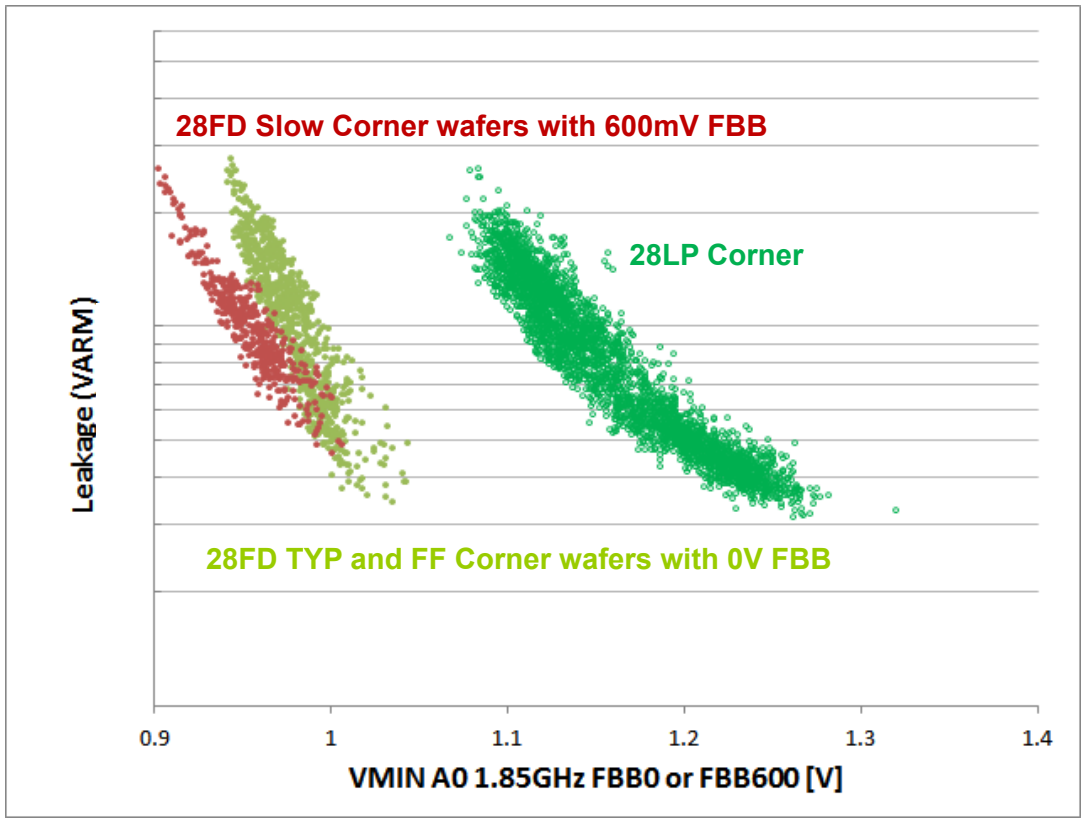
- AVS (Adaptive Voltage Scaling) compensates global process variations adapting the supply voltage
- FBB acts on transistor Vt, allowing a “true” process compensation
  - Allowing asymmetric compensation of Nmos and Pmos
  - Allowing easy different compensations by block
    - Large SoC may be partitioned, each one having its own compensation
      - Managing multiple BB generators is easier than multiple supply voltages
- FBB enables advanced compensation techniques (R&D)
  - Temperature tracking & compensation
  - BTI (aging) compensation

Cortex A9™ Benchmark 28nm Silicon Results



- VMIN for a given frequency (1.85GHz)
  - Vmin search is an EWS metric for Fmax
  - The metric allows a one-to-one benchmark between 28FD and 28LP performances

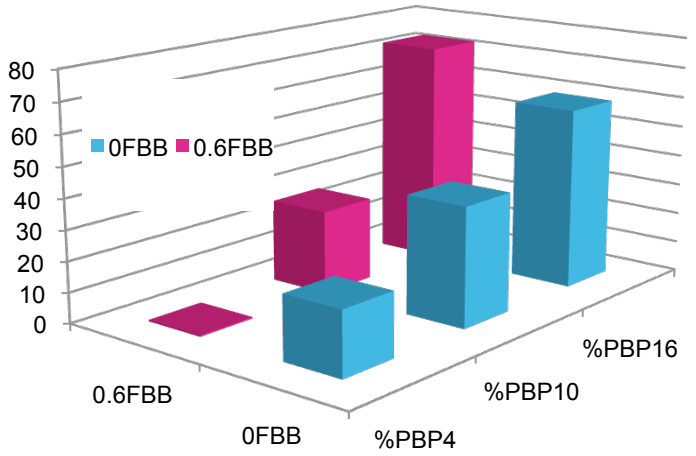
Cortex A9™ Benchmark Process Compensation through FBB



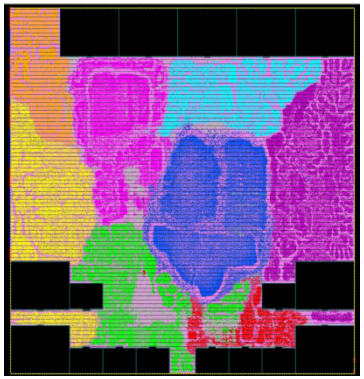
- Applying FBB 600mV enable reaching the target VMIN perfs
  - SLOW Population brought in TT-FF range

Process compensation through FBB benefits at implementation level

- ARM Processor
  - 350 Kgates, 50k FF + memories
  - Target frequency: 1GHz @ WC/0.85V
- Two FD-SOI implementations comparison
  - Standard WC methodology
  - SS corner compensated with 600mV FBB



Sign-off	Standard	With Process Compensation
Area (µm²)	1	0.90x
Total Power (mW) @ Vmax, 125C, RCmax	1	0.75x
Leakage (mA) @ Vmax, 125C	1	0.7x



FD-SOI & Multiprocessing

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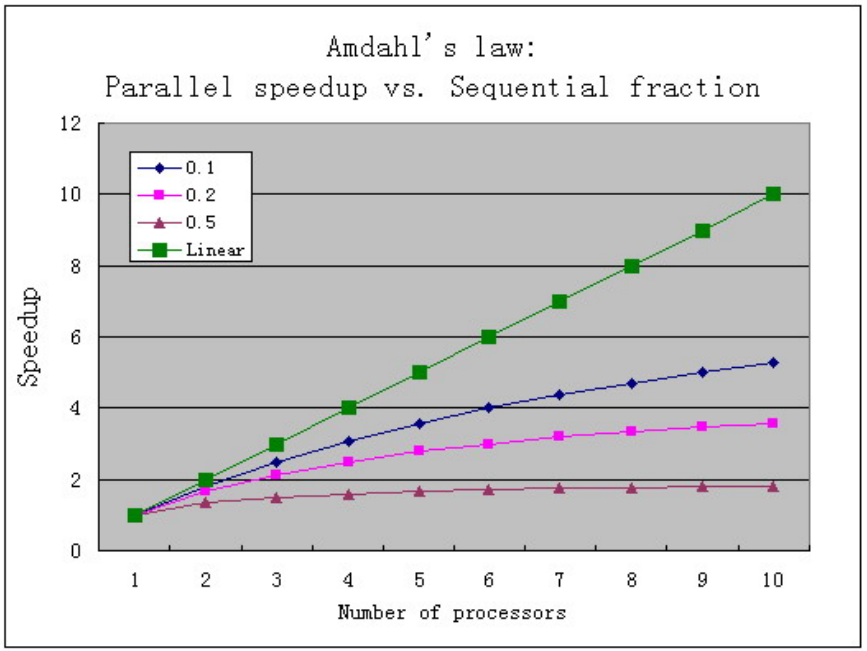
Multicore Delivers more MIPS/mW

- No doubt multicore can deliver more MIPS per mW
  - Core should be implemented for best power efficiency/peak frequency trade-off
  - SoC should host as many cores as possible at every technology node
    - scalability achieved through core number increase
    - no more by frequency scaling
- Major issues
  - Amdahl's law
  - Memory hierarchy efficiency



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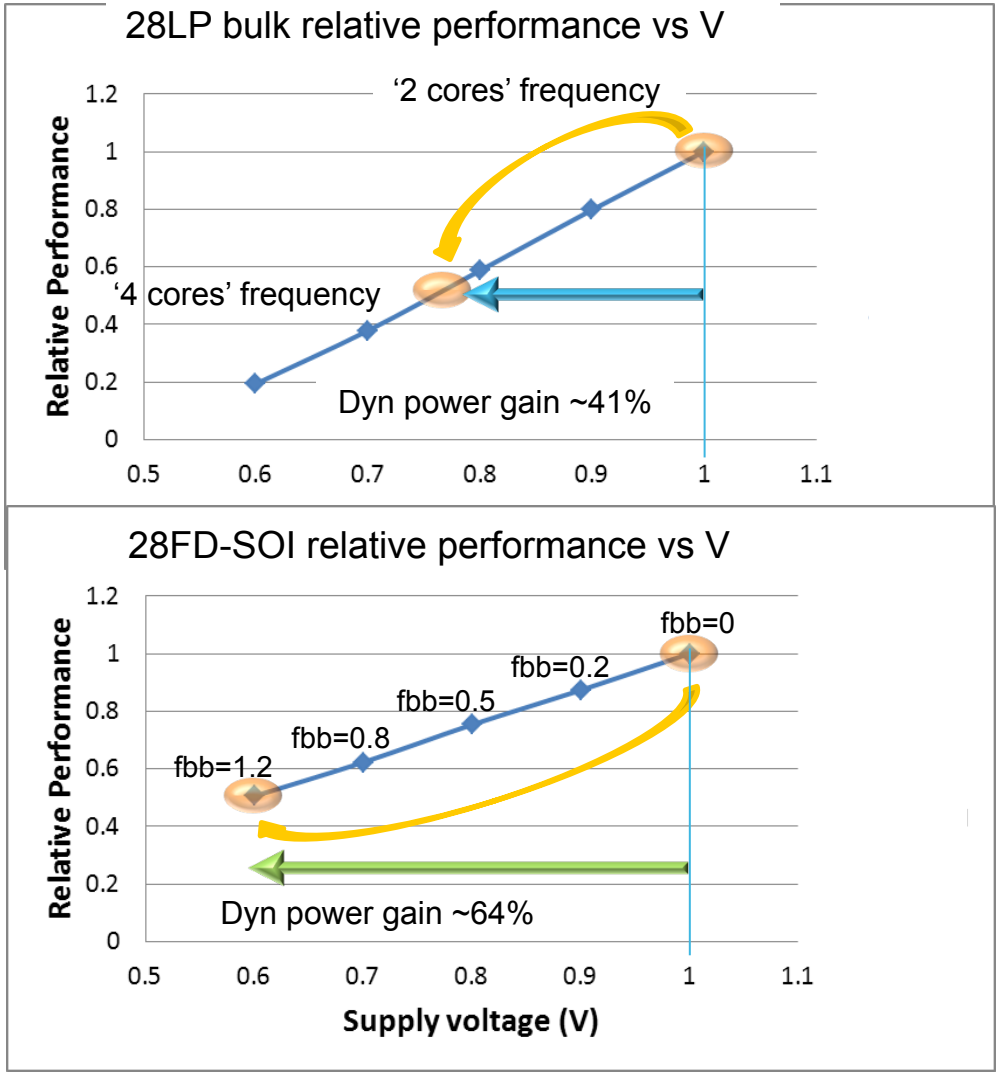
Multiprocessing and wide DVFS - 1

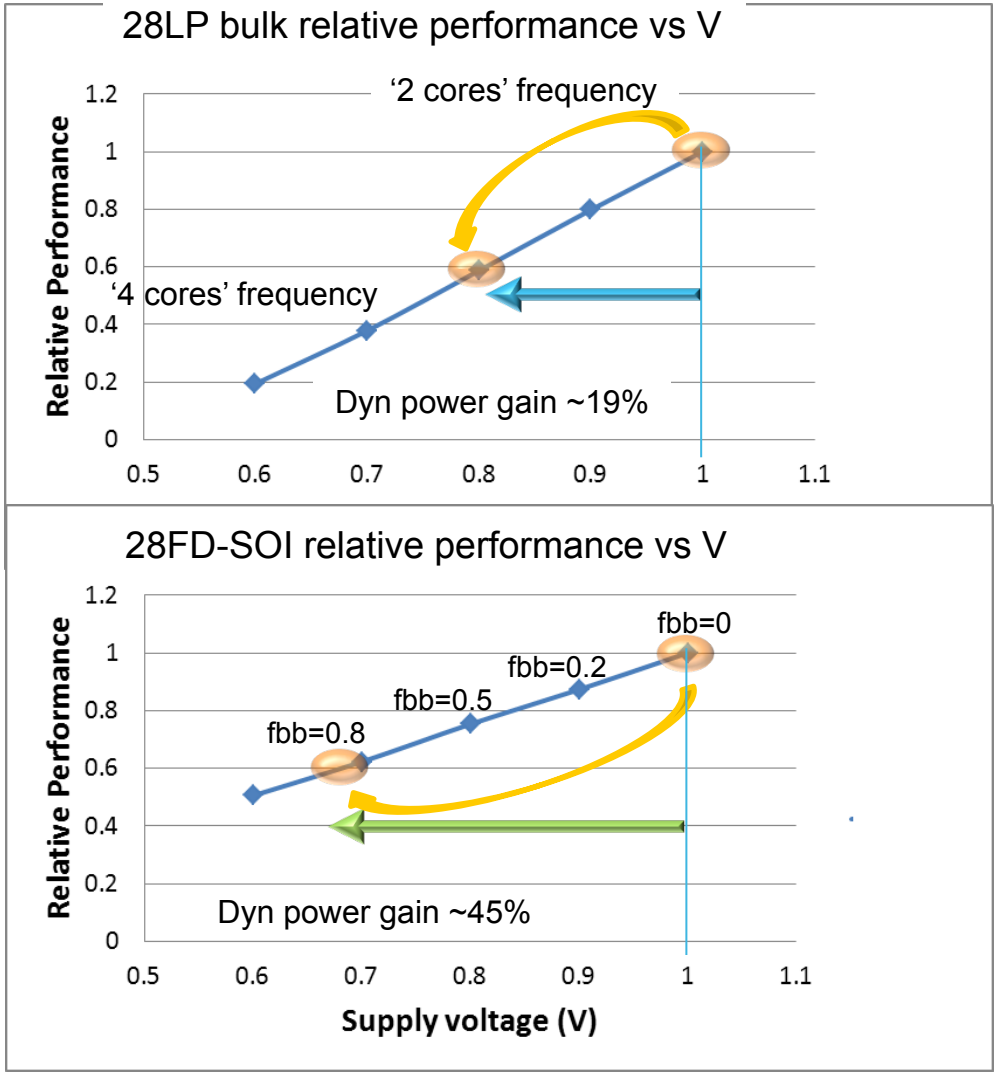
- 2 cores vs 4 cores
  - Ideal speed up factor
  - 2 cores@F=4 cores@F/2



D.Jacquet et al., VLSI Symposium 2013

Multiprocessing and wide DVFS - 2

- 2 cores vs 4 cores
  - Seq fraction = 0.1
  - 2 cores@F=4 cores@0.6F



D.Jacquet et al., VLSI Symposium 2013

FD-SOI and Ultra Low Power / Voltage applications

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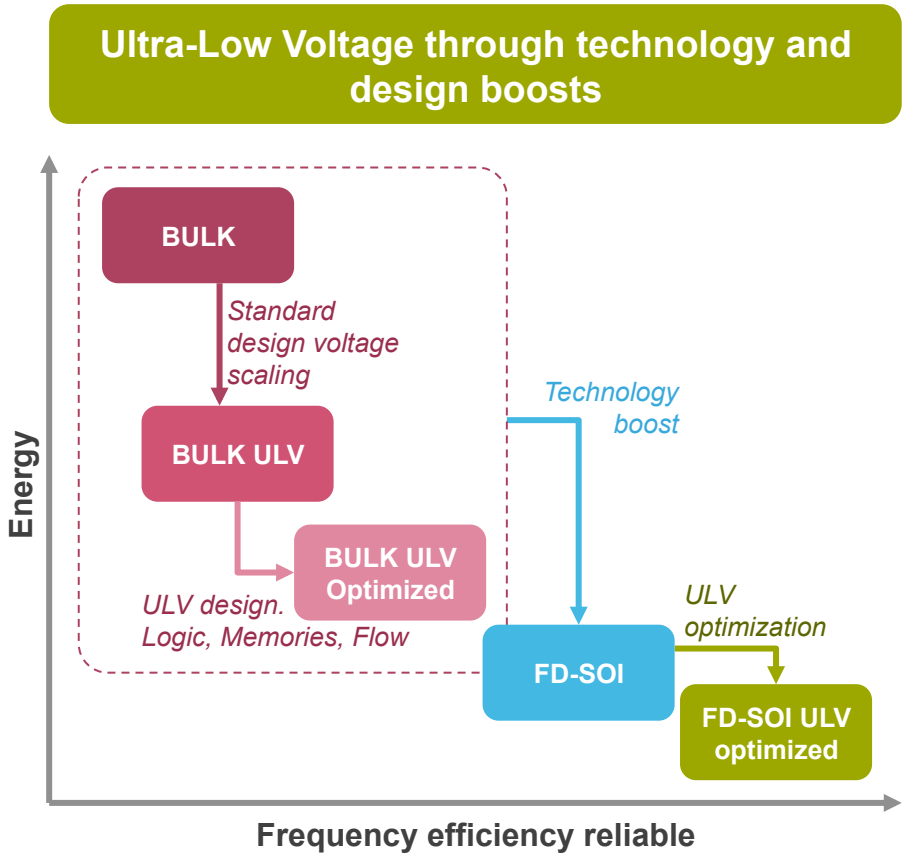
ULV Gains Confirmed in 28 FD-SOI

- Intrinsic FD-SOI advantage for ULV
  - Electrostatic control enhancement

  → speed at low voltage
  - Undoped homogeneous channel

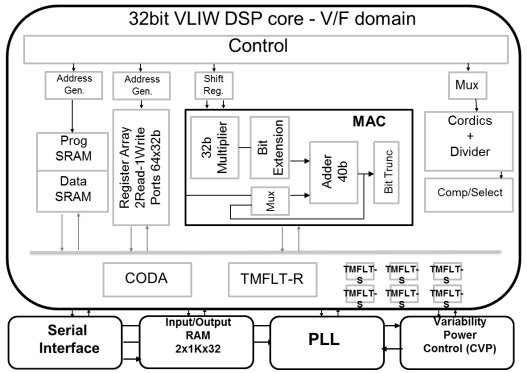
  → Reduced variability

  → Lower minimum usable supply voltage
- Specific design solutions to leverage FDSOI outstanding performance at ULV
  - Higher I_{ON} for clock tree
  - FBB for improved energy efficiency and delay

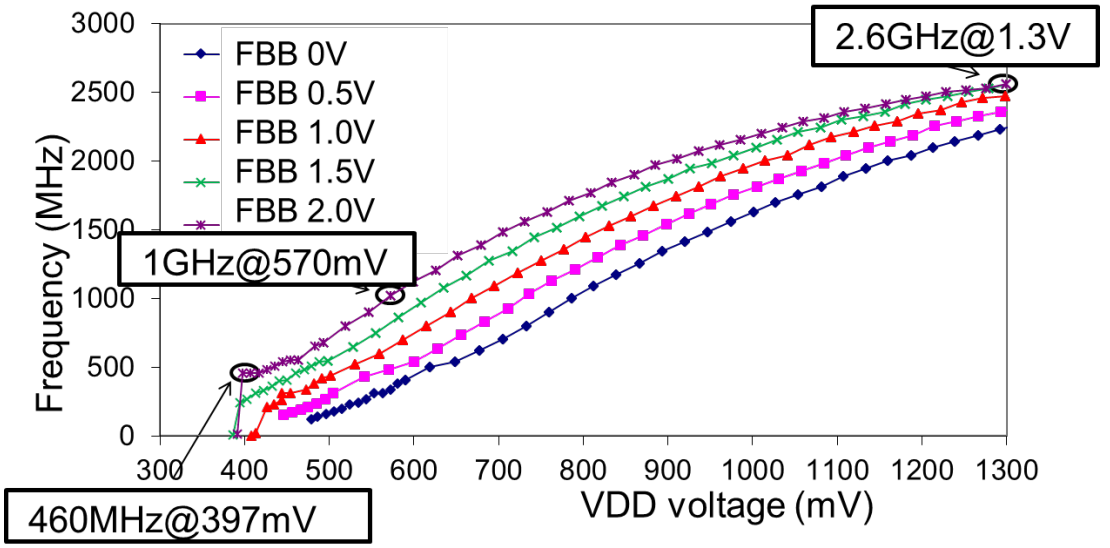


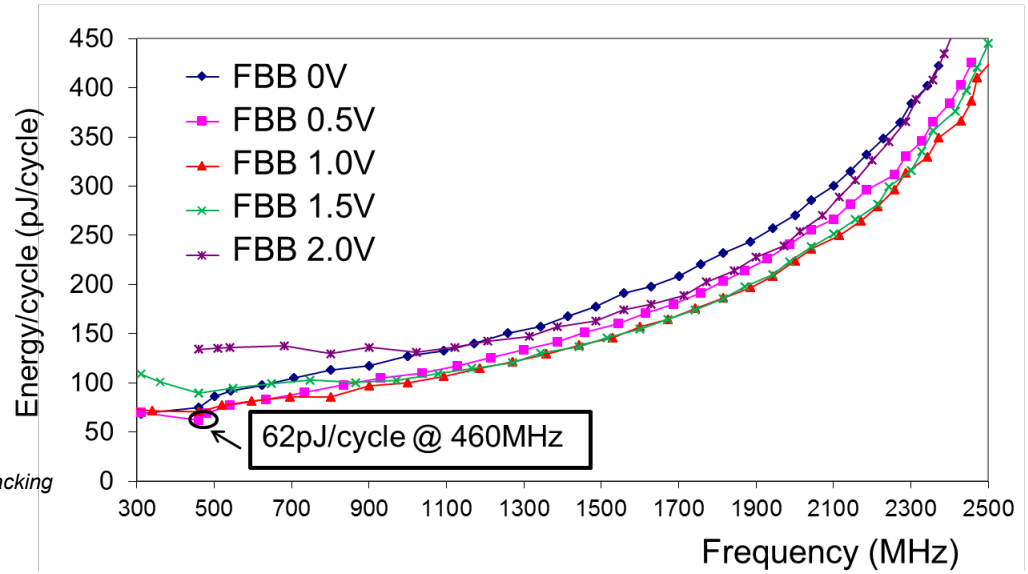
Example: ULV DSP

- FBB up to +2V and FMAX tracking :
  - ↗ frequency up to 460MHz at minimum voltage



- For a fixed voltage supply :
  - Lowest energy at 460MHz
  - Power consumption : 370mW at 1V





27.1 : A 460MHz@397mV – 2.6GHz@1.3V 32bit VLIW DSP Embedding FMAX Tracking

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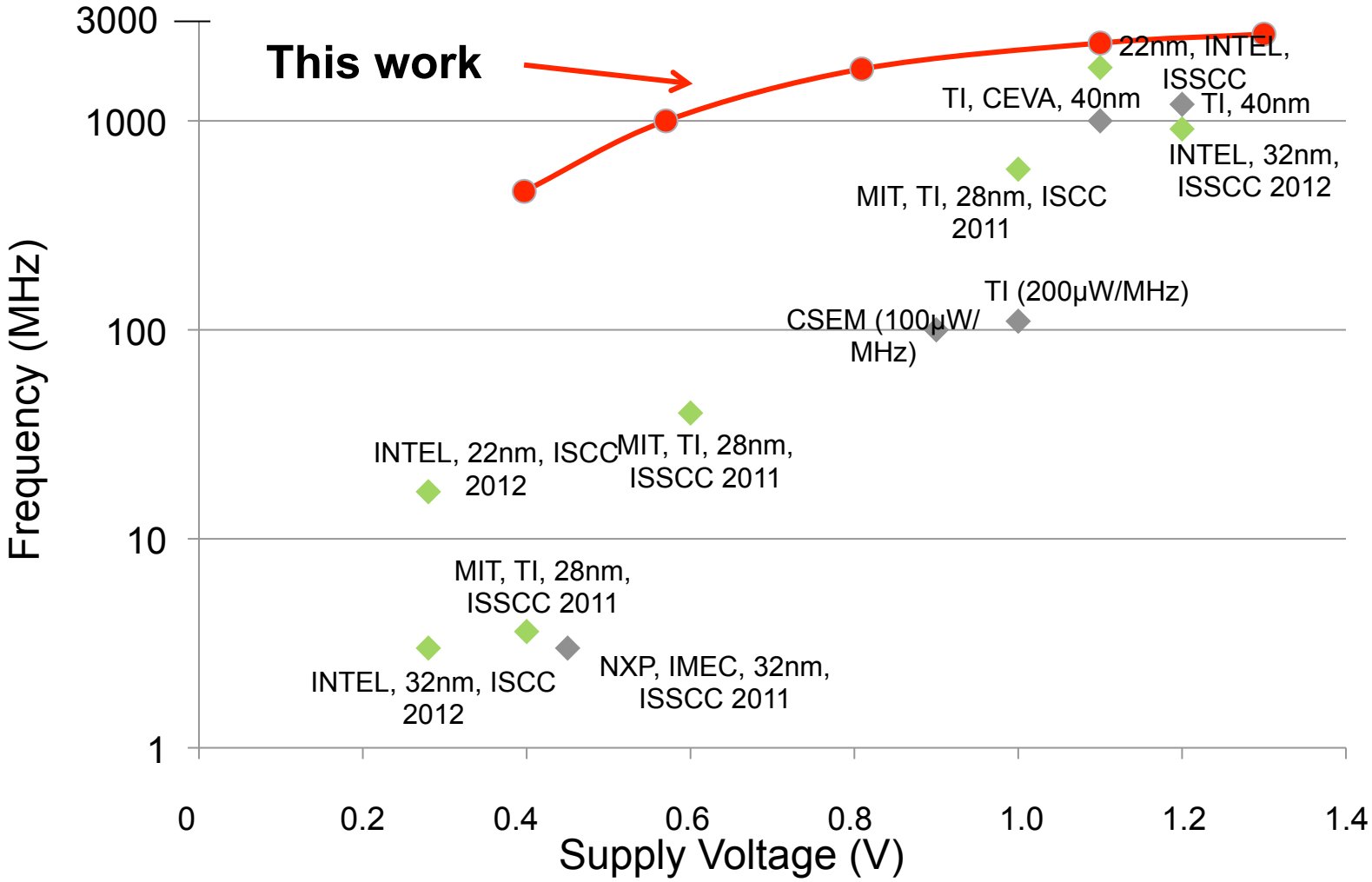
Comparison with State of the Art WVR



27.1 : A 460MHz@397mV – 2.6GHz@1.3V 32bit VLIW DSP Embedding FMAX Tracking

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Thank You!